74ABT2240

Octal inverting buffer with 30 Ω series termination resistors; 3-state

Rev. 04 — 17 January 2005 Product data sheet

1. General description

The 74ABT2240 high performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT2240 device is an octal inverting buffer that is ideal for driving bus lines. The device features two output enable inputs ($1\overline{OE}$ and $2\overline{OE}$), each controlling four of the 3-state outputs.

The 74ABT2240 is designed with 30 Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

The 74ABT2240 is the same as the 74ABT240. The part number has been changed to reflect industry standards.

2. Features

- Octal bus interface
- 3-state buffers
- Live insertion and extraction permitted
- Outputs include series resistance of 30 Ω, making external termination resistors unnecessary
- Output capability: +12 mA and –32 mA
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V
- Power-up 3-state
- Same part as 74ABT240

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay nAn to n$\overline{Y}$n	C_L = 50 pF; V_{CC} = 5 V	-	2.8	-	ns
t_{PHL}	propagation delay nAn to n$\overline{Y}$n	C_L = 50 pF; V_{CC} = 5 V	-	4.3	-	ns
C_I	input capacitance	V_I = 0 V or V_{CC}	-	3	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or V_{CC}	-	7	-	pF
I_{CC}	quiescent supply current	outputs 3-state; V_{CC} = 5 V	-	50	-	μA

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT2240N	–40 °C to +85 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74ABT2240D	–40 °C to +85 °C	S020	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT2240PW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

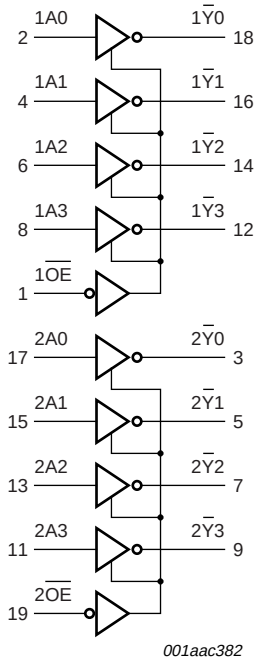


Fig 1. Logic symbol

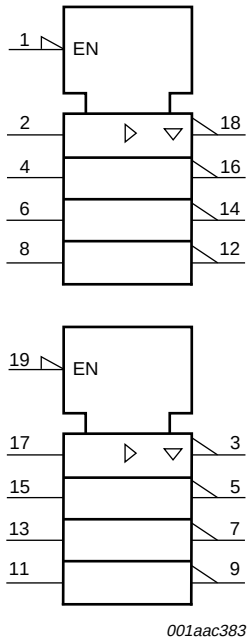


Fig 2. IEC logic symbol

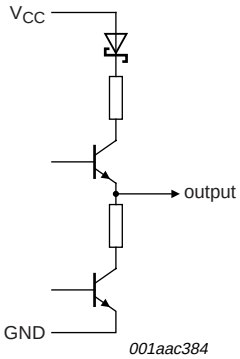


Fig 3. Logic diagram one output

6. Pinning information

6.1 Pinning

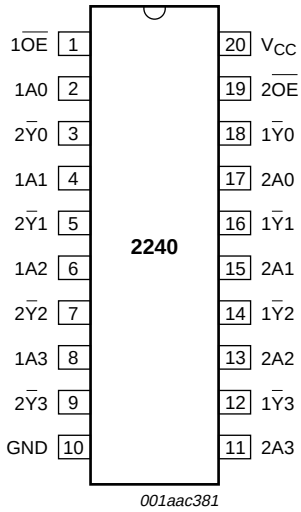


Fig 4. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1$\overline{OE}$	1	outputs 1 enable control input
1A0	2	data input
2$\overline{Y}$0	3	data output
1A1	4	data input
2$\overline{Y}$1	5	data output
1A2	6	data input
2$\overline{Y}$2	7	data output
1A3	8	data input
2$\overline{Y}$3	9	data output
GND	10	ground (0 V)
2A3	11	data input
1$\overline{Y}$3	12	data output
2A2	13	data input
1$\overline{Y}$2	14	data output
2A1	15	data input
1$\overline{Y}$1	16	data output
2A0	17	data input

Table 3: Pin description *…continued*

Symbol	Pin	Description
$1\overline{Y}0$	18	data output
$2\overline{OE}$	19	outputs 2 enable control input
V_{CC}	20	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Control input	Input	Output
$n\overline{OE}$	nAn	$n\overline{Y}n$
L	L	H
L	H	L
H	X	Z

[1] H = HIGH voltage;
L = LOW voltage;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+5.5	V
I_{IK}	input diode current	$V_I < 0$ V		–18	-	mA
I_{OK}	output diode current	$V_O < 0$ V		–50	-	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	–32	mA
I_{OL}	LOW-level output current		-	-	12	mA
$\Delta t/\Delta V$	input transition rise or fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
V_{IK}	input diode voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	–0.9	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		2.5	2.9	-	V
		I_{OH} = –32 mA		2.0	2.4	-	V
		V_{CC} = 5.0 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		3.0	3.4	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_{OL} = 5 mA		-	0.32	0.55	V
		I_{OL} = 12 mA		-	-	0.8	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	±0.01	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_O or V_I 4.5 V		-	±5.0	±100	µA
I_{PU}, I_{PD}	power-up or power-down down 3-state output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{nOE} = don't care	[1]	-	±5.0	±50	µA
I_{OZ}	3-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}					
		output HIGH-state at V_O = 2.7 V		-	0.01	50	µA
		output LOW-state at V_O = 0.5 V		-	–0.01	–50	µA
I_{CEX}	output HIGH-state leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[2]	–50	–100	–180	mA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}					
		outputs HIGH-state		-	50	250	µA
		outputs LOW-state		-	24	30	mA
		outputs 3-state		-	50	250	µA
ΔI_{CC}	additional supply current						
	per data input pin	one data input at 3.4 V and other inputs at V_{CC} or GND; V_{CC} = 5.5 V	[3]				
		outputs enabled		-	0.5	1.5	mA
		outputs 3-state		-	0.5	1.5	mA
	per enable input pin	one enable input at 3.4 V and other inputs at V_{CC} or GND; V_{CC} = 5.5 V	[3]				
		outputs 3-state		-	0.5	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}		-	3	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or V_{CC}		-	7	-	pF

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C							
V_{IK}	input diode voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	-	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		2.5	-	-	V
		I_{OH} = –32 mA		2.0	-	-	V
		V_{CC} = 5.0 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		3.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_{OL} = 5 mA		-	-	0.55	V
		I_{OL} = 12 mA		-	-	0.8	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0.0 V; V_O or $V_I \leq$ 4.5 V		-	-	±100	µA
I_{PU}, I_{PD}	power-up or power-down down 3-state output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{nOE} = don't care	[1]	-	-	±50	µA
I_{OZ}	3-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}					
		output HIGH-state at V_O = 2.7 V		-	-	50	µA
		output LOW-state at V_O = 0.5 V		-	-	–50	µA
I_{CEX}	output HIGH-state leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		-	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[2]	–50	-	–180	mA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}					
		outputs HIGH-state		-	-	250	µA
		outputs LOW-state		-	-	30	mA
		outputs 3-state		-	-	250	µA
ΔI_{CC}	additional supply current						
	per data input pin	one data input at 3.4 V and other inputs at V_{CC} or GND; V_{CC} = 5.5 V	[3]				
		outputs enabled		-	-	1.5	mA
		outputs 3-state		-	-	1.5	mA
	per enable input pin	one enable input at 3.4 V and other inputs at V_{CC} or GND; V_{CC} = 5.5 V	[3]				
		outputs 3-state		-	-	1.5	mA

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 % a transition time of up to 100 µs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

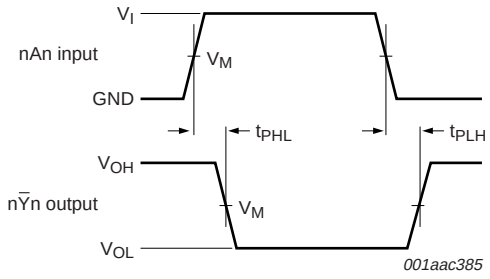
11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PLH}	propagation delay nAn to $\overline{nY}n$	V_{CC} = 5 V; see Figure 5	1.0	2.8	4.0	ns
t_{PHL}	propagation delay nAn to $\overline{nY}n$	V_{CC} = 5 V; see Figure 5	3.0	4.3	5.8	ns
t_{PZH}	output enable time to HIGH-level	V_{CC} = 5 V; see Figure 6	1.5	3.4	4.7	ns
t_{PZL}	output enable time to LOW-level	V_{CC} = 5 V; see Figure 6	3.5	5.5	7.6	ns
t_{PHZ}	output disable time from HIGH-level	V_{CC} = 5 V; see Figure 6	1.9	4.1	5.0	ns
t_{PLZ}	output disable time from LOW-level	V_{CC} = 5 V; see Figure 6	2.5	3.4	5.8	ns
T_{amb} = −40 °C to +85 °C						
t_{PLH}	propagation delay nAn to $\overline{nY}n$	V_{CC} = 5 V ± 0.5 V; see Figure 5	1.0	-	4.9	ns
t_{PHL}	propagation delay nAn to $\overline{nY}n$	V_{CC} = 5 V ± 0.5 V; see Figure 5	3.0	-	6.0	ns
t_{PZH}	output enable time to HIGH-level	V_{CC} = 5 V ± 0.5 V; see Figure 6	1.5	-	5.8	ns
t_{PZL}	output enable time to LOW-level	V_{CC} = 5 V ± 0.5 V; see Figure 6	3.5	-	8.4	ns
t_{PHZ}	output disable time from HIGH-level	V_{CC} = 5 V ± 0.5 V; see Figure 6	1.9	-	5.6	ns
t_{PLZ}	output disable time from LOW-level	V_{CC} = 5 V ± 0.5 V; see Figure 6	2.5	-	6.4	ns

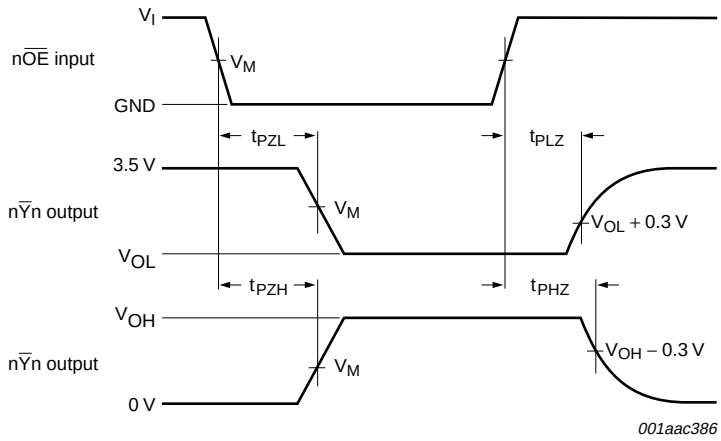
12. Waveforms



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

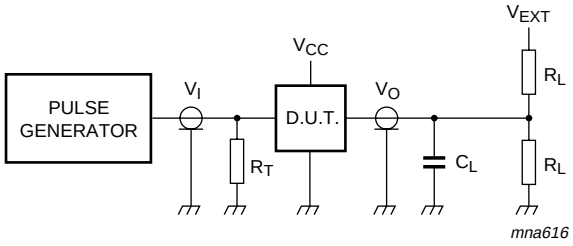
Fig 5. Propagation delays of input (nAn) to output ($\overline{nY}n$)



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 6. Enable and disable times of 3-state outputs



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

V_{EXT} = Test voltage for switching times.

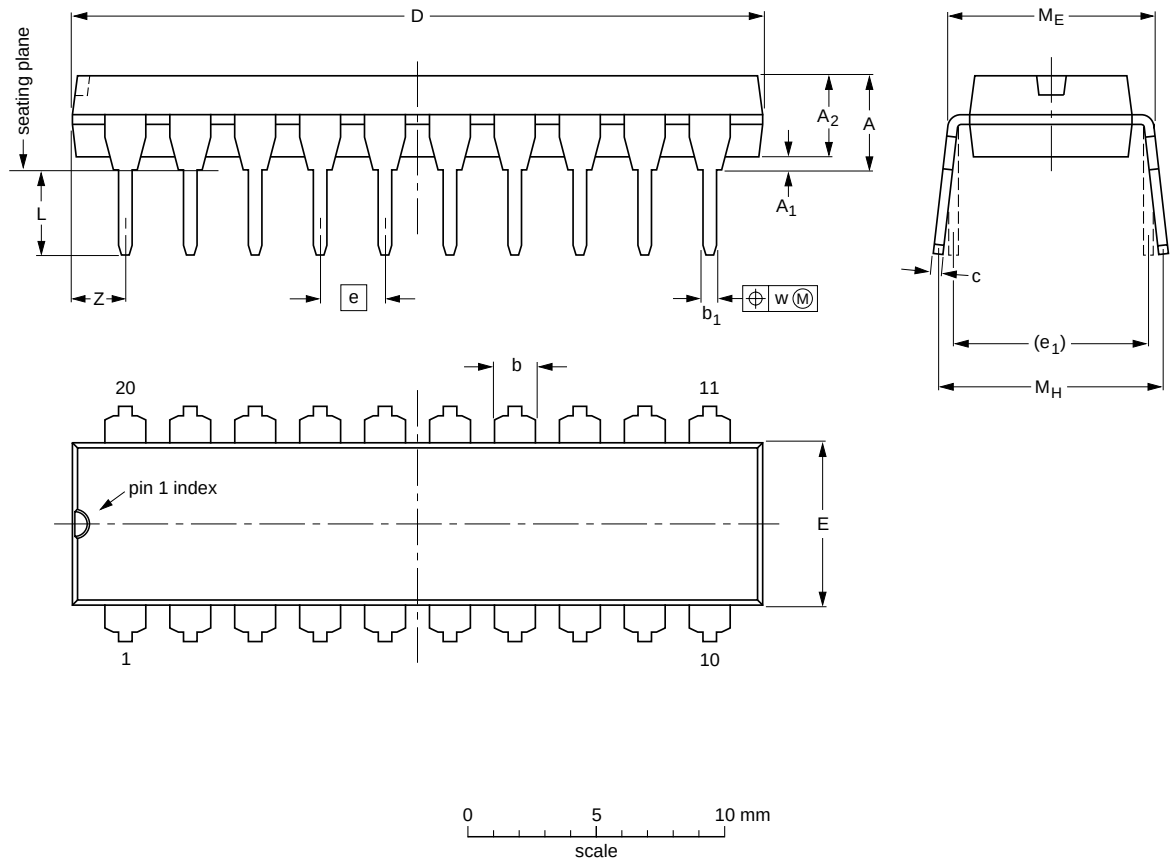
Fig 7. Test circuit for 3-state outputs

Table 9: Test data

Input		Load		V_{EXT}		
V_I	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3 V	2.5 ns	50 pF	500 Ω	open	7 V	open

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

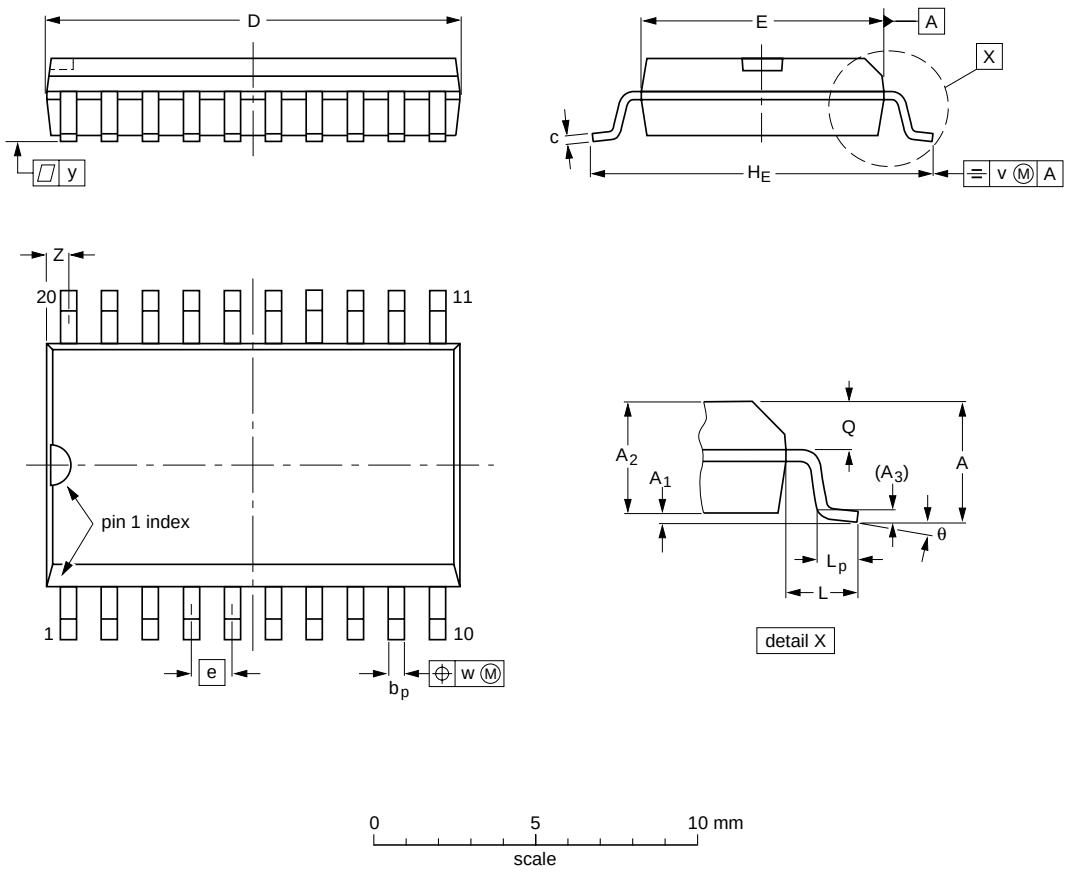
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 8. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

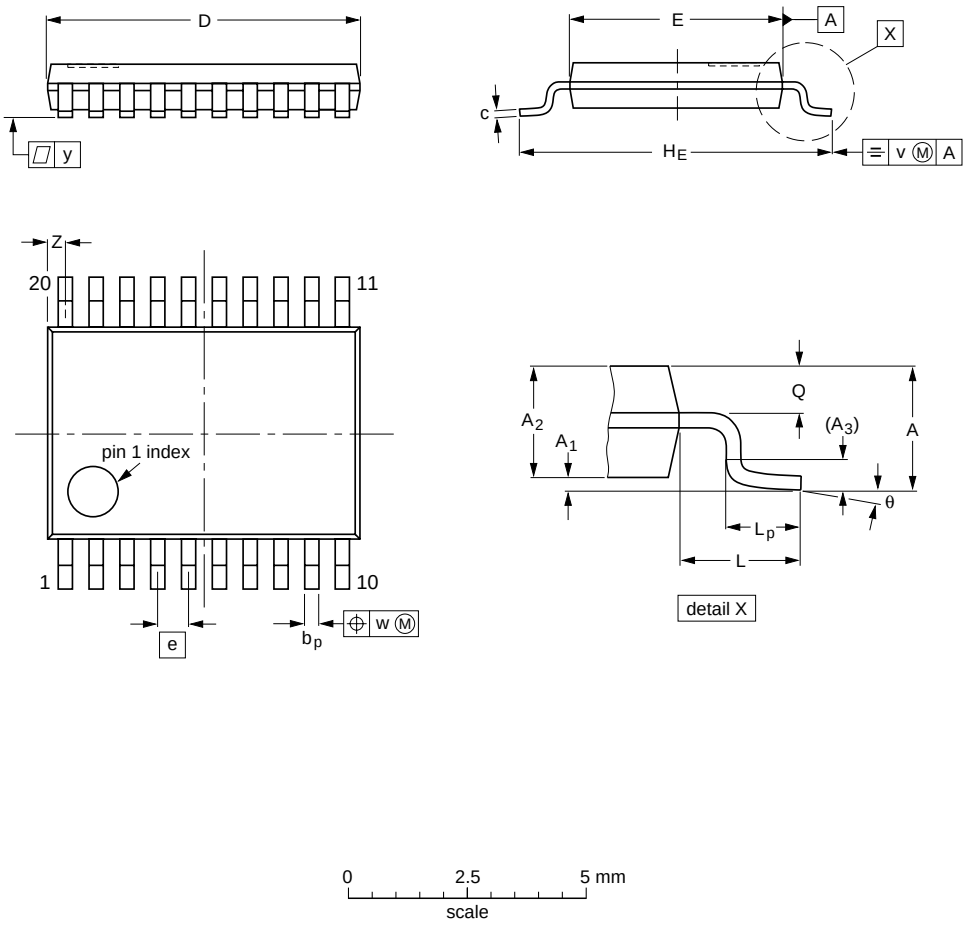
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT360-1 (TSSOP20)

14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ABT2240_4	20050117	Product data sheet	-	9397 750 14414	74ABT2240_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 2 “Features”: modified ‘JEDEC Std. 17’ into ‘JESD78’. • Table 8 “Dynamic characteristics”: changed min value of t_{PZL} from 4.2 ns into 3.5 ns for both conditions V_{CC} = 5.0 V at T_{amb} = 25 °C and V_{CC} = 5.0 V ± 0.5 V at T_{amb} = –40 °C to +85 °C.				
74ABT2240_3	20030425	Product specification	ECN 853-1626 29854	9397 750 11431	74ABT2240_2
74ABT2240_2	19980116	Product specification	ECN 853-1626 18865	9397 750 03463	74ABT2240_1
74ABT2240_1	19961008	Product specification	-	-	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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18. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

19. Contents

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