

## PIC16(L)F722A/723A Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F722A/723A family devices that you have received conform functionally to the current Device Data Sheet (DS41417B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC16(L)F722A/723A silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on [page 4](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site ([www.microchip.com](http://www.microchip.com)).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
  - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
  - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon (  )
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F722A/723A silicon revisions are shown in [Table 1](#).

**TABLE 1: SILICON DEVREV VALUES**

Part Number	Device ID <sup>(1)</sup>	Revision ID for Silicon Revision <sup>(2)</sup>		
		A2	A3	A4
PIC16F722A	01 1011 001x xxxx	0x2	0x3	0x4
PIC16LF722A	01 1011 011x xxxx	0x2	0x3	0x4
PIC16F723A	01 1011 000x xxxx	0x2	0x3	0x4
PIC16LF723A	01 1011 010x xxxx	0x2	0x3	0x4

- Note 1:** The Device ID is located at 2006h. The five Least Significant bits comprise the revision ID.
- 2:** Refer to the “*PIC16(L)F72X Memory Programming Specification*” (DS41332) for detailed information on Device and Revision IDs for your specific device.

# PIC16(L)F722A/723A

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**TABLE 2: SILICON ISSUE SUMMARY**

Module	Feature	Item Number	Issue Summary	Affected Revisions		
				A2	A3	A4
<a href="#">Oscillator</a>	External HS Oscillator	<a href="#">1.1</a>	Operation below 2.7V.	X		
<a href="#">Interrupts</a>	Stack Push	<a href="#">2.1</a>	Interrupt logic incorrectly pushes two addresses to the stack.	X	X	X

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

### 1. Module: Oscillator

#### 1.1 Operation below 2.7V

The minimum device VDD when using the external crystal oscillator in HS mode is 3.0V.

#### Work around

Use the internal oscillator or an external clock source if operating below the 3.0V required for HS mode.

#### Affected Silicon Revisions

A2	A3	A4					
X							

### 2. Module: Interrupts

2.1 The interrupt logic incorrectly pushes two addresses to the stack when vectoring to the interrupt vector. Specifically, the interrupt vector address 0x4 is incorrectly pushed to the stack after the current PC, at the time the interrupt was received, is pushed. This will cause the stack to overflow if the user program is operating seven calls deep when an interrupt arrives. Because the stack is circular, the overflow causes the first stack address to be overwritten.

#### Work around

Disable interrupts by clearing the GIE bit in the INTCON register whenever the user program is operating seven calls deep. This ensures that interrupts will not cause the stack to overflow.

#### Affected Silicon Revisions

A2	A3	A4					
X	X	X					

# PIC16(L)F722A/723A

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41417B).

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 1. Module: DC Characteristics

In Section 23.2, the maximum values for D015 parameter have been modified as shown below.

### 23.2 DC Characteristics: PIC16(L)F22A/723A-I/E (Industrial, Extended)

PIC16LF722A/723A		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
PIC16F722A/723A		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
<b>Supply Current (IDD)<sup>(1, 2)</sup></b>							
D014		—	290	330	μA	1.8	Fosc = 4 MHz
		—	460	500	μA	3.0	EC Oscillator mode
D014		—	300	430	μA	1.8	Fosc = 4 MHz
		—	450	655	μA	3.0	EC Oscillator mode ( <b>Note 5</b> )
		—	500	730	μA	5.0	
D015		—	100	<b>155</b>	μA	1.8	Fosc = 500 kHz
		—	120	<b>175</b>	μA	3.0	MFINTOSC mode
D015		—	115	195	μA	1.8	Fosc = 500 kHz
		—	135	200	μA	3.0	MFINTOSC mode ( <b>Note 5</b> )
		—	150	220	μA	5.0	
D016		—	650	800	μA	1.8	Fosc = 8 MHz
		—	1000	1200	μA	3.0	HFINTOSC mode
D016		—	625	850	μA	1.8	Fosc = 8 MHz
		—	1000	1200	μA	3.0	HFINTOSC mode ( <b>Note 5</b> )
		—	1100	1500	μA	5.0	
D017		—	1.0	1.2	mA	1.8	Fosc = 16 MHz
		—	1.5	1.85	mA	3.0	HFINTOSC mode
D017		—	1	1.2	mA	1.8	Fosc = 16 MHz
		—	1.5	1.7	mA	3.0	HFINTOSC mode ( <b>Note 5</b> )
		—	1.7	2.1	mA	5.0	

- Note 1:** The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.
- Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
- Note 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula  $I_R = V_{DD}/2R_{EXT}$  (mA) with REXT in kΩ.
- Note 4:** FVR and BOR are disabled.
- Note 5:** 0.1 μF capacitor on VCAP (RA0).

## APPENDIX A: DOCUMENT REVISION HISTORY

### **Rev. A Document (07/2010)**

Initial release of this document.

### **Rev. B Document (02/2011)**

Updated errata to new format; Added Module 2, Interrupts.

### **Rev. C Document (01/2012)**

Added Silicon Revision A4.

### **Rev. D Document (02/2014)**

Data Sheet Clarifications: Added Module 1; Other minor corrections.

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