FEMTOCLOCK™ CRYSTAL/LVCMOS-TO-3.3V LVPECL/LVCMOS SYNTHESIZER

ICS843001I-23

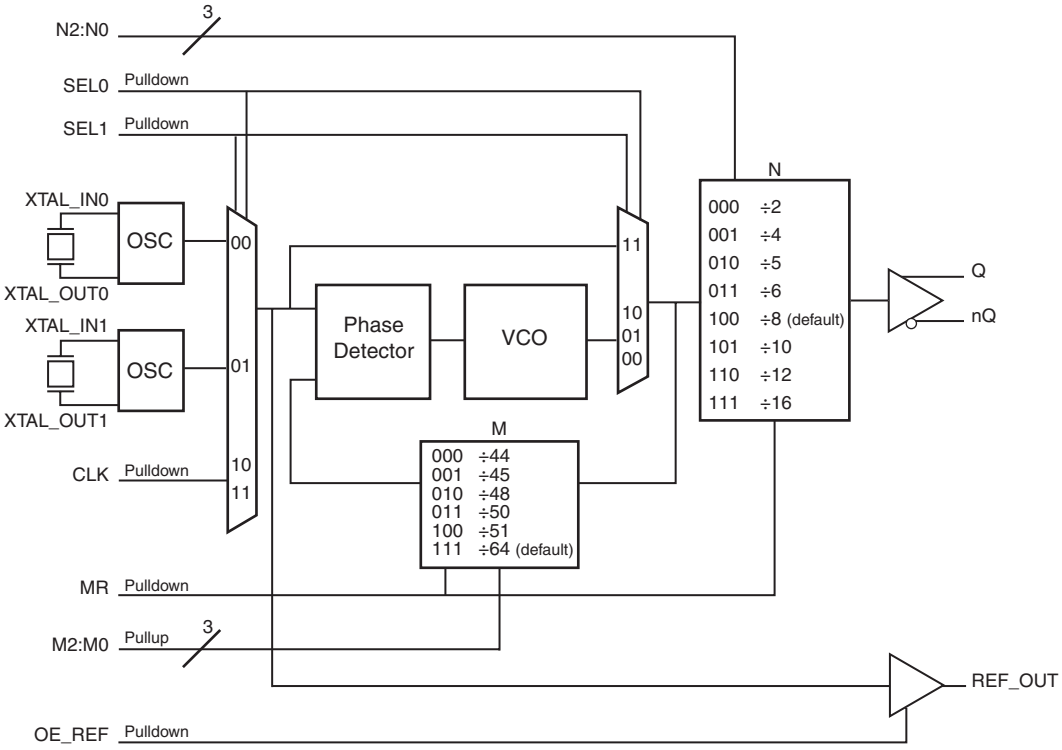
General Description

The ICS843001I-23 is a highly versatile, low phase noise LVPECL/LVCMOS Synthesizer which can generate low jitter reference clocks for a variety of communication applications and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. The dual crystal interface allows the synthesizer to support up to three communication standards in a given application (i.e. SONET with a 19.44MHz crystal, 1Gb/10Gb Ethernet and Fibre Channel using a 25MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET, GbE/10Gb Ethernet and SAN applications. The ICS843001I-23 is packaged in a small 24-pin TSSOP package.

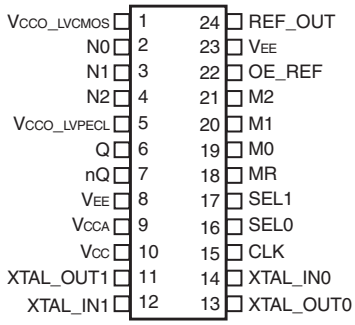
Features

- One 3.3V LVPECL output pair and one LVCMOS/LVTTL REF_OUT output
- Selectable crystal oscillator interfaces or LVCMOS/LVTTL single-ended input
- Crystal and CLK range: 17.5MHz - 29.54MHz
- Able to generate GbE/10GbE/12GbE, Fibre Channel (1Gb/4Gb/10Gb), PCI-E and SATA from a 25MHz crystal
- VCO range: 1.12GHz - 1.3GHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): 0.9ps (typical) @ 3.3V
- Supply modes:
  V_{CC}/V_{CCO}
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS843001I-23
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{CCO_CMOS}	Power		Output supply pin for LVCMOS/LVTTL REF_OUT output.
2, 3	N0, N1	Input	Pulldown	Output divider select pins. See Table 3C. LVCMOS/LVTTL interface levels.
4	N2	Input	Pullup	
5	V_{CCO_LVPECL}	Power		Output supply pin for LVPECL output.
6, 7	Q, nQ	Ouput		Differential output pair. LVPECL interface levels.
8, 23	V_{EE}	Power		Negative supply pin.
9	V_{CCA}	Power		Analog supply pin.
10	V_{CC}	Power		Core supply pin.
11 12	XTAL_OUT1, XTAL_IN1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
13 14	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
15	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
16, 17	SEL0, SEL1	Input	Pulldown	Input MUX select pins. LVCMOS/LVTTL interface levels.
18	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output nQ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
19, 20 , 21	M0, M1, M2	Input	Pullup	Feedback divider select pins. See Table 3B. LVCMOS/LVTTL interface levels.
22	OE_REF	Input	Pulldown	Reference clock output enable. Default Low. See Table 3E. LVCMOS/LVTTL interface levels.
24	REF_OUT	Output		Reference clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance					pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{out}	Output Impedance	REF_OUT		20		Ω

TABLE 3A. COMMON CONFIGURATIONS TABLE

Input XTAL Input (MHz)	Feedback Divider	VCO (MHz)	N Divider Value	Output Frequency (MHz)	Application
27	44	1188	16	74.25	HDTV
24.75	48	1188	16	74.25	HDTV
19.44	64	1244.16	8	155.52	SONET
19.44	64	1244.16	2	622.08	SONET
19.44	64	1244.16	4	311.04	SONET
25	50	1250	10	125	GigE
25	50	1250	8	156.25	10 GigE
25	50	1250	5	250	GigE
25	50	1250	4	312.5	XGMII
25	50	1250	2	625	10 GigE
25	45	1125	6	187.5	12 GigE
25	48	1200	12	100	PCI Express
25	48	1200	8	150	SATA
25	48	1200	16	75	SATA
25	51	1275	12	106.25	Fibre Channel
25	51	1275	8	159.375	10 Gig Fibre Channel
25	51	1275	6	212.5	4 Gig Fibre Channel

TABLE 3B. PROGRAMMABLE M OUTPUT DIVIDER FUNCTION TABLE

Inputs			M Divider Value	Input Frequency	
M2	M1	M0		Minimum	Maximum
0	0	0	44	25.5	29.54
0	0	1	45	24.9	28.88
0	1	0	48	23.3	27.08
0	1	1	50	22.4	26.0
1	0	0	51	22.0	25.49
1	1	1	64 (default)	17.5	20.31

TABLE 3C. PROGRAMMABLE N OUTPUT DIVIDER FUNCTION TABLE

Inputs			N Divide Value
N2	N1	N0	
0	0	0	2
0	0	1	4
0	1	0	5
0	1	1	6
1	0	0	8 (default)
1	0	1	10
1	1	0	12
1	1	1	16

TABLE 3D. BYPASS MODE FUNCTION TABLE

Inputs		Reference Input	PLL Mode
SEL1	SEL0		
0	0	XTAL0	Active
0	1	XTAL1	Active
1	0	CLK	Active
1	1	CLK	Bypass

TABLE 3E. OE_REF OUTPUT FUNCTION TABLE

Inputs	Output
OE_REF	REF_OUT
0	Hi-Z
1	Active

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO_LVCMOS} + 0.5V
Package Thermal Impedance, θ_{JA}	82.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_LVPECL}, V_{CCO\_LVCMOS}$ = 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.05	3.3	V_{CC}	V
V_{CCO_LVPECL}	Output Supply Voltage		3.135	3.3	3.465	V
V_{CCO_LVCMOS}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			105		mA
I_{CCA}	Analog Supply Current			5		mA
I_{CCO}	Output Supply Current			5		mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, $V_{CCO\_LVPECL}, V_{CCO\_LVCMOS}$ = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.05	3.3	V_{CC}	V
V_{CCO_LVPECL}	Output Supply Voltage		2.375	2.5	2.625	V
V_{CCO_LVCMOS}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			105		mA
I_{CCA}	Analog Supply Current			5		mA
I_{CCO}	Output Supply Current			5		mA

Table 4C. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_LVPECL}, V_{CCO\_LVCMOS}$ = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.05	2.5	V_{CC}	V
V_{CCO_LVPECL}	Output Supply Voltage		2.375	2.5	2.625	V
V_{CCO_LVCMOS}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			100		mA
I_{CCA}	Analog Supply Current			5		mA
I_{CCO}	Output Supply Current			5		mA

TABLE 4D. LVCMOS / LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	CLK, SEL0, SEL1, OE_REF, MR, N0, N1	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
		N2, M0:M2	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK, SEL0, SEL1, OE_REF, MR, N0, N1	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		N2, M0:M2	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1	REF_OUT	V_{CCO_LVCMOS} = 3.465V	2.6			V
			V_{CCO_LVCMOS} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	REF_OUT	V_{CCO_LVCMOS} = 3.465V or 2.625V			0.5	V
ΔV/ΔT	Input Edge Rate	CLK	20% - 80%			TBD	V/ns

NOTE 1: Output terminated with 50Ω to V_{CCO_LVCMOS}/2. See Parameter Measurement Information Section, "Output Load Test Circuit Diagram" diagrams.

TABLE 4E. LVPECL DC CHARACTERISTICS, V_{CC} = V_{CCO_LVPECL} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_LVPECL} - 1.4		V_{CCO_LVPECL} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_LVPECL} - 2.0		V_{CCO_LVPECL} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_LVPECL} - 2V.

TABLE 4F. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5% or 2.5V±5%, V_{CCO_LVPECL} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_LVPECL} - 1.4		V_{CCO_LVPECL} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_LVPECL} - 2.0		V_{CCO_LVPECL} - 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_LVPECL} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			MHz
Frequency		17.5		29.54	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVPECL}, V_{CCO\_LVCMOS}$ = 3.3V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			56		650	MHz
t_{PD}	Propagation Delay, NOTE 1	CLK to REF_OUT			2.5		ns
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 2, 3		622.08MHz (12kHz - 20MHz)		0.9		ps
f_{VCO}	PLL VCO Lock Range			1.12		1.3	GHz
$tL_{\_SEL}$	Select Time						ms
$tL_{\_M}$	PLL Lock Time						ms
t_R / t_F	Output Rise/Fall Time	Q/nQ	20% to 80%		300		ps
		REF_OUT	20% to 80%		500		ps
odc	Output Duty Cycle	Q/nQ			50		%
		REF_OUT			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the V_{CC}/2 of the input to V_{CCO_LVCMOS}/2 of the output.
NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, $V_{CCO\_LVPECL}, V_{CCO\_LVCMOS}$ = 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			56		650	MHz
t_{PD}	Propagation Delay, NOTE 1	CLK to REF_OUT			3.5		ns
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 2, 3		622.08MHz (12kHz - 20MHz)		1		ps
f_{VCO}	PLL VCO Lock Range			1.12		1.3	GHz
$tL_{\_SEL}$	Select Time						ms
$tL_{\_M}$	PLL Lock Time						ms
t_R / t_F	Output Rise/Fall Time	Q/nQ	20% to 80%		300		ps
		REF_OUT	20% to 80%		500		ps
odc	Output Duty Cycle	Q/nQ			50		%
		REF_OUT			50		%

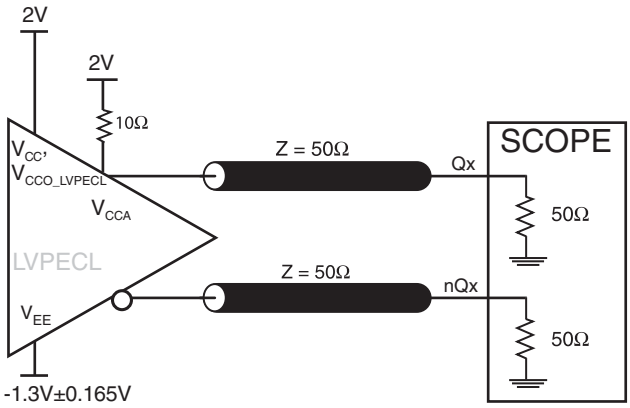
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the V_{CC}/2 of the input to V_{CCO_LVCMOS}/2 of the output.
NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6C. AC CHARACTERISTICS, $V_{CC} = V_{CCO\_LVPECL}$, V_{CCO_LVCMOS} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C TO 85°C

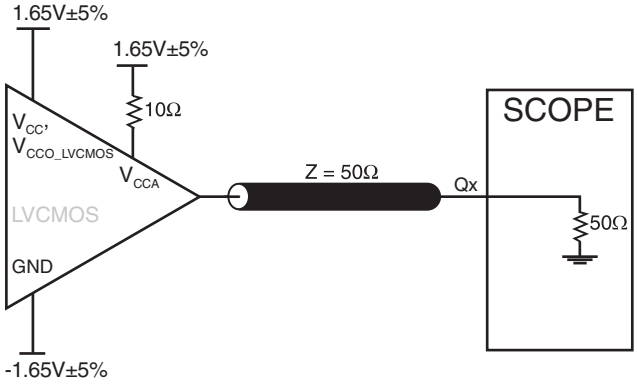
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			56		650	MHz
t_{PD}	Propagation Delay, NOTE 1	CLK to REF_OUT			3		ns
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 2, 3		622.08MHz (12kHz - 20MHz)		1.1		ps
f_{VCO}	PLL VCO Lock Range			1.12		1.3	GHz
$tL_{\_SEL}$	Select Time						ms
$tL_{\_M}$	PLL Lock Time						ms
t_R / t_F	Output Rise/Fall Time	Q/nQ	20% to 80%		300		ps
		REF_OUT	20% to 80%		500		ps
odc	Output Duty Cycle	Q/nQ			50		%
		REF_OUT			50		%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the V_{CC}/2 of the input to V_{CCO_LVCMOS}/2 of the output.
NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

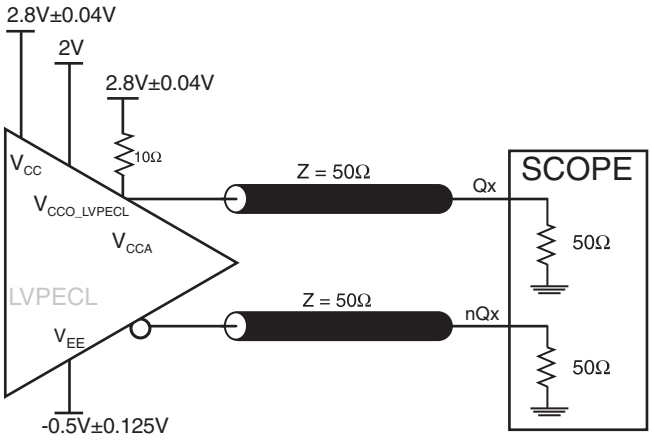
Parameter Measurement Information



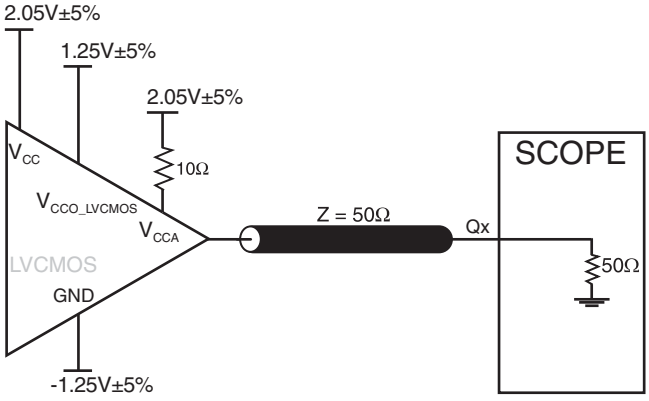
3.3V LVPECL Output Load AC Test Circuit



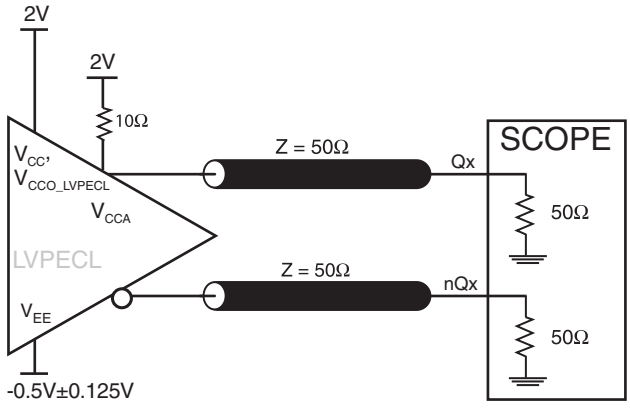
3.3V LVCMOS Output Load AC Test Circuit



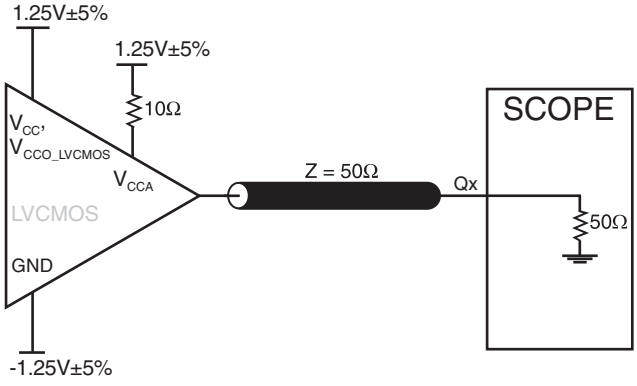
3.3V Core/2.5V LVPECL Output Load AC Test Circuit



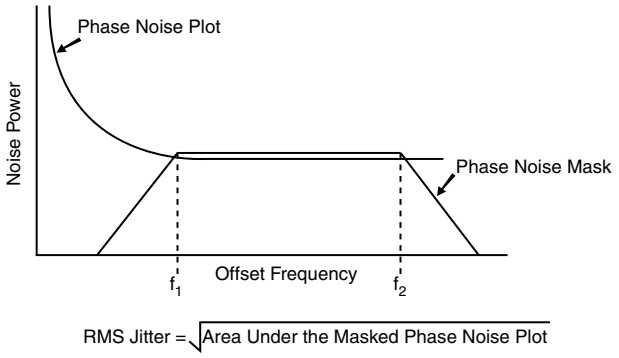
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



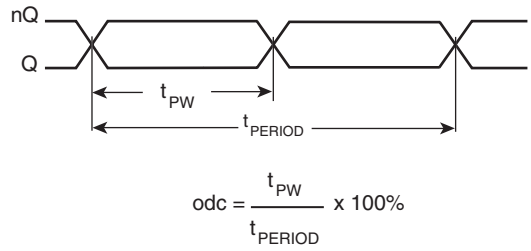
2.5V LVPECL Output Load AC Test Circuit



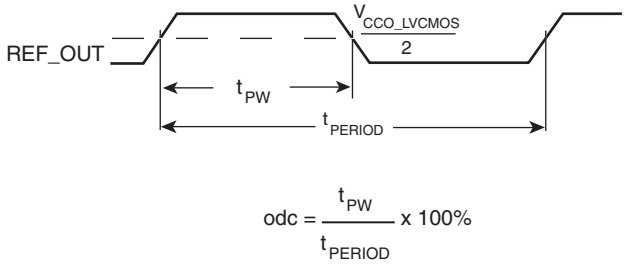
2.5V LVCMOS Output Load AC Test Circuit



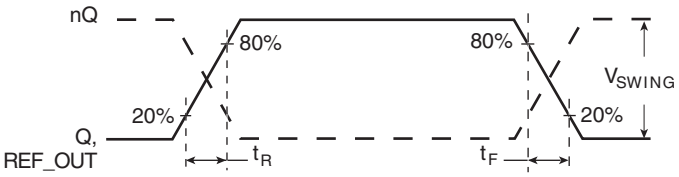
RMS Phase Jitter



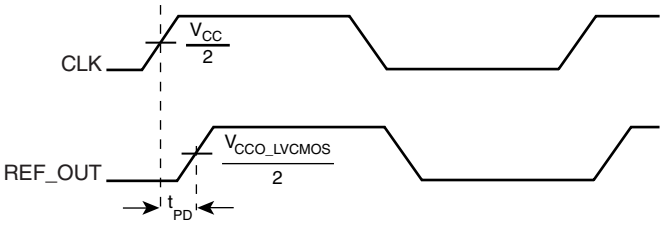
LVPECL Output Duty Cycle/Pulse Width/Period



LVCMOS Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



Propagation Delay

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843001I-23 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_X} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

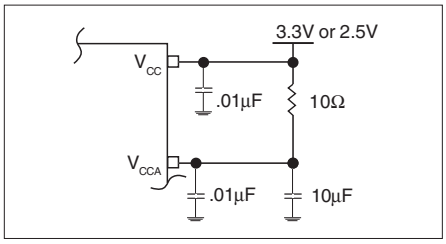


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK INPUT

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS CONTROL PINS

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT

The unused LVCMOS output can be left floating. There should be no trace attached.

LVPECL OUTPUT

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS843001I-23 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

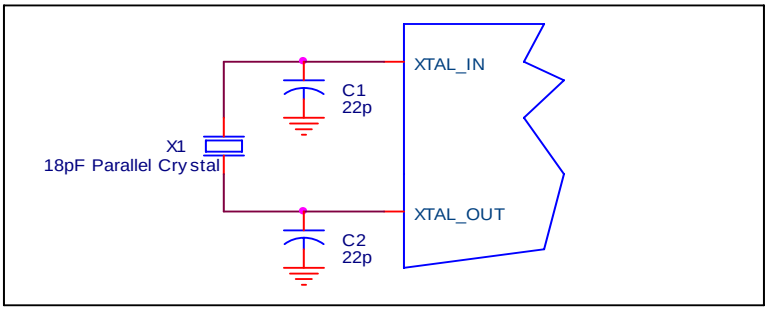


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

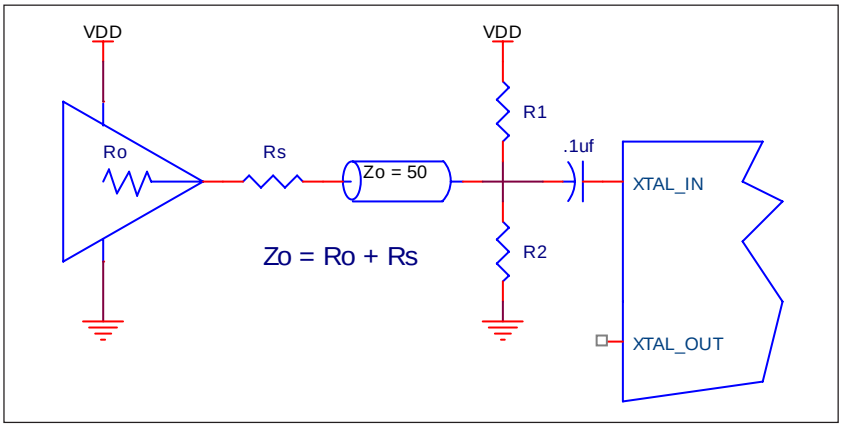


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

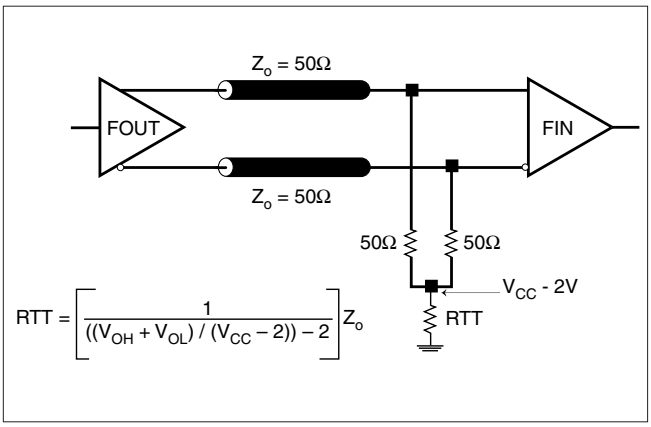


FIGURE 4A. LVPECL OUTPUT TERMINATION

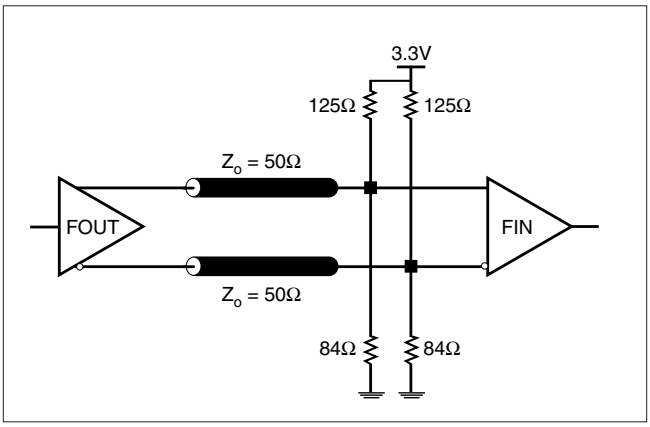


FIGURE 4B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

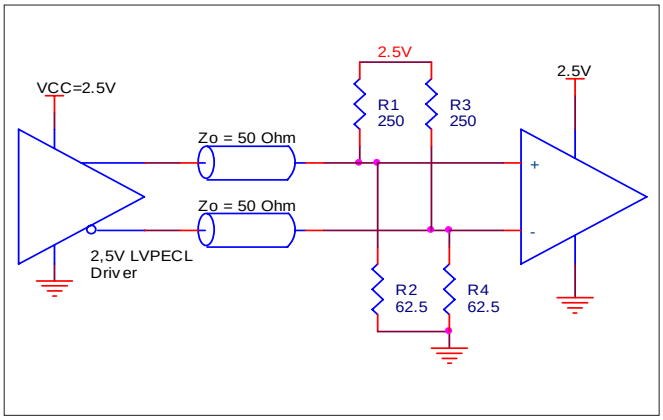


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

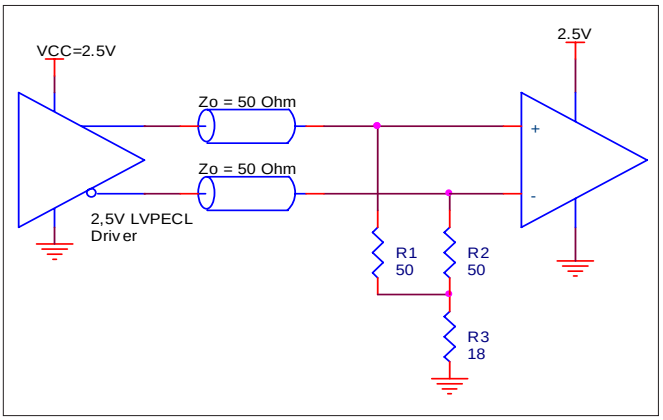


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

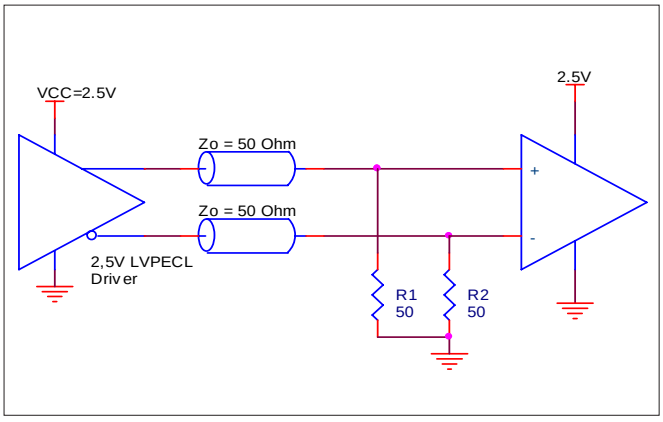


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843001I-23.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843001I-23 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 105mA = **363.8mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{_MAX}$ **(3.465V, with all outputs switching) = 363.8mW + 30mW = 393.8**mW

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.3°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.394W * 82.3°C/W = 117.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*

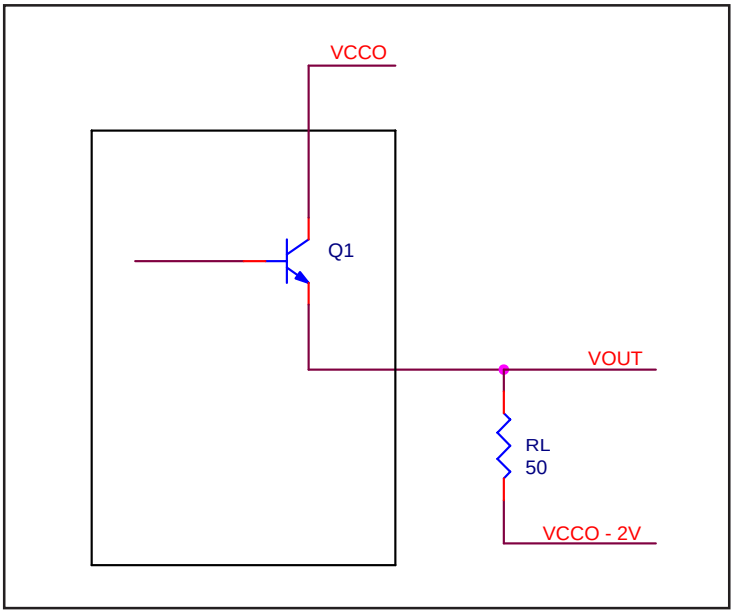


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

Transistor Count

The transistor count for ICS843001I-23 is: 4165

Package Outline and Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

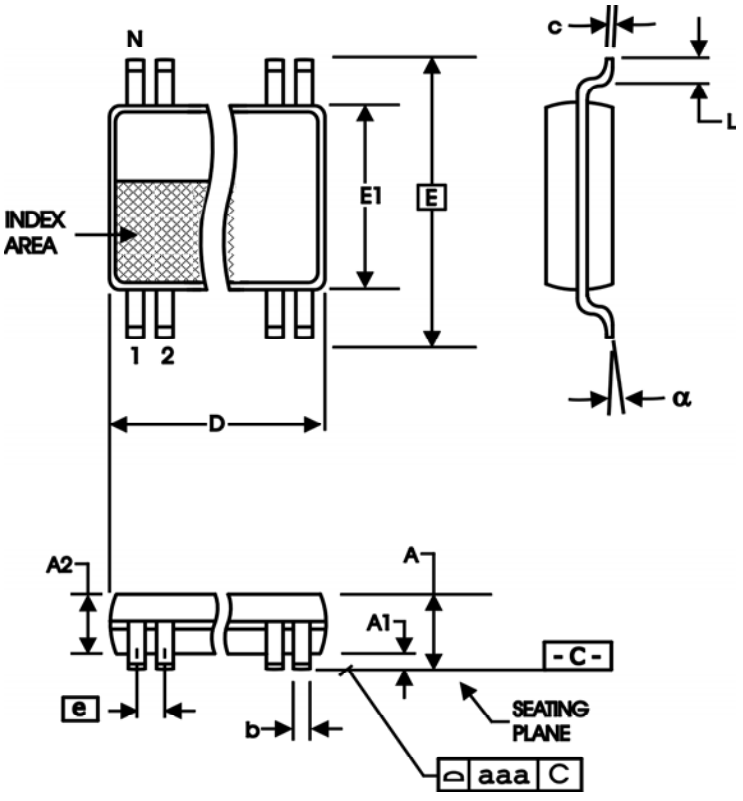


Table 9. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843001BGI-23	ICS843001BI23	24 Lead TSSOP	tube	-40°C to 85°C
843001BGI-23T	ICS843001BI23	24 Lead TSSOP	2500 tape & reel	-40°C to 85°C
843001BGI-23LF	ICS43001BI23L	24 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
843001BGI-23LFT	ICS43001BI23L	24 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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