

CEC1702 Silicon Errata and Data Sheet Clarification

TABLE 1: SILICON IDENTIFICATION

Part Number	Silicon Identifier	Functional Revision C
CEC1702	Device ID ⁽¹⁾	31h
	Revision ID for Silicon Revision ⁽²⁾	02h
	PIS ⁽³⁾ Version/Revision	C1
Note 1: The Device ID is visible as an 8-bit number at Plug and Play Configuration Index 20h. 2: The HW Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 21h. 3: Product Identification System (PIS) is defined in the Product Data Sheet.		

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾
				C
SMB Controller	SMB Master	1.	SMBus Master Controller violates Bus Idle Time between STO and STA in Byte mode only	X
JTAG Pins	Pins	2.	GPIO145 & GPIO146 input disabled in SWD mode	X
Note 1: Only those issues indicated in the last column apply to the current silicon revision.				

Silicon Errata Issues

1. Module: SMBus 2.0 Host Controller

DESCRIPTION

SMBus Master Controller violates Bus Idle Time between STO and STA in Byte mode only. This issue only occurs in a multi-master environment.

Under firmware control, it is possible to generate a new command on the bus before the Bus Idle time expires, thereby violating the SMBus Idle time.

END USER IMPLICATIONS

The SMBus Master Controller may generate a START condition too soon. The two consequences of this scenario are that another master will issue a transaction that will get corrupted, which is handled by the lost arbitration mechanism, or the CEC1702 master will unfairly claim the bus too often.

Work Around

There are two solutions:

- Use the Network Layer instead of Byte mode. This anomaly does not apply to the SMBus Network Layer operation.
- If firmware polls the nBB bit to indicate not busy before asserting the PIN bit and writing the data register, the SMBus Controller will not violate the Bus Idle time.

2. Module: GPIO145 and GPIO146 Inputs Disabled When JTAG Enabled

DESCRIPTION

GPIO145 and GPIO146 inputs are disabled when JTAG enabled and the JTAG debugger is connected in both 4-wire JTAG mode and 2-wire SWD mode.

END USER IMPLICATIONS

- Cannot use SMB09 when JTAG is enabled and JTAG debugger is connected if device is configured for 2-wire SWD test mode.
- Cannot use GPIO145 and GPIO146 inputs when JTAG is enabled and JTAG debugger is connected if device is configured for 2-wire SWD test mode.

Work Around

None.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet.

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

TABLE 3: DATA SHEET CLARIFICATION SUMMARY

Module	Item Number	Issue Summary
WDT	1.	WDT_STATUS bit is Reserved

1. Module: WDT

This section clarifies which WDT status bit must be used for detecting watchdog timer events.

WDT TIMER EVENTS

The WDT_STATUS bit documented in the WDT Control register is a Reserved bit and cannot be used to detect watchdog timer events.

Bit[5] WDT located in the Power-Fail and Reset Status register in the VBAT Register Bank must be used as the WDT Status bit.

CEC1702

APPENDIX A: DOCUMENT REVISION HISTORY

REVISION	DESCRIPTION
DS80000723A (01-30-17)	Initial release

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