

# NTHC5513

## Power MOSFET

20 V, +3.9 A / -3.0 A,  
Complementary ChipFET™

### Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD Package Featuring Complementary Pair
- ChipFET Package Provides Great Thermal Characteristics Similar to Larger Packages
- Low  $R_{DS(on)}$  in a ChipFET Package for High Efficiency Performance
- Low Profile (< 1.10 mm) Allows Placement in Extremely Thin Environments Such as Portable Electronics
- Pb-Free Package is Available

### Applications

- Load Switch Applications Requiring Level Shift
- DC-DC Conversion Circuits
- Drive Small Brushless DC Motors
- Designed for Power Management Applications in Portable, Battery Powered Products

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit		
Drain-to-Source Voltage			$V_{DSS}$	20	V		
Gate-to-Source Voltage			$V_{GS}$	$\pm 12$	V		
Continuous Drain Current (Note 1)	N-Ch Steady State	$T_A = 25^\circ\text{C}$	$I_D$	2.9	A		
		$T_A = 85^\circ\text{C}$		2.1			
	$t \leq 5$	$T_A = 25^\circ\text{C}$		3.9			
		$T_A = 85^\circ\text{C}$		-1.6			
	P-Ch Steady State	$T_A = 25^\circ\text{C}$		$I_D$		-2.2	A
		$T_A = 85^\circ\text{C}$				-1.6	
$t \leq 5$	$T_A = 25^\circ\text{C}$	-3.0					
	Pulsed Drain Current (Note 1)		$I_{DM}$		12	A	
N-Ch	$t = 10 \mu\text{s}$	-9.0					
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$		1.1	W	
		$T_A = 25^\circ\text{C}$		2.1			
		$t \leq 5$		$T_A = 25^\circ\text{C}$	2.1		
Operating Junction and Storage Temperature			$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$		
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			$T_L$	260	$^\circ\text{C}$		

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

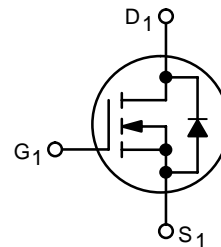
1. Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



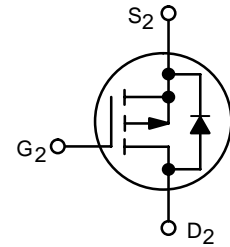
ON Semiconductor®

<http://onsemi.com>

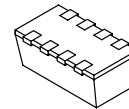
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
N-Channel 20 V	60 m $\Omega$ @ 4.5 V	3.9 A
	80 m $\Omega$ @ 2.5 V	
P-Channel -20 V	130 m $\Omega$ @ -4.5 V	-3.0 A
	200 m $\Omega$ @ -2.5 V	



N-Channel MOSFET

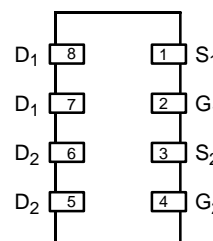


P-Channel MOSFET

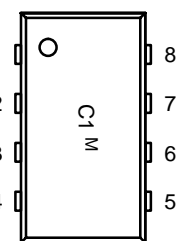


ChipFET  
CASE 1206A  
STYLE 2

### PIN CONNECTIONS



### MARKING DIAGRAM



C1 = Specific Device Code  
M = Month Code

### ORDERING INFORMATION

Device	Package	Shipping†
NTHC5513T1	ChipFET	3000/Tape & Reel
NTHC5513T1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTHC5513

## THERMAL RESISTANCE RATINGS

Parameter		Symbol	Max	Unit
Junction-to-Ambient (Note 1)	Steady State	$R_{\theta JA}$	110	°C/W
	$t \leq 5$		60	

2. Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
-----------	--------	-----	-----------------	-----	-----	-----	------

### OFF CHARACTERISTICS (Note 3)

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N	$V_{GS} = 0\text{ V}$	$I_D = 250\ \mu\text{A}$	20		V
		P		$I_D = -250\ \mu\text{A}$	-20		
Zero Gate Voltage Drain Current	$I_{DSS}$	N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$			1.0	$\mu\text{A}$
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$			-1.0	
		N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}, T_J = 85^\circ\text{C}$			5	
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}, T_J = 85^\circ\text{C}$			-5	
Gate-to-Source Leakage Current	$I_{GSS}$		$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	$I_D = 250\ \mu\text{A}$	0.6	1.2	V
		P		$I_D = -250\ \mu\text{A}$	-0.6	-1.2	
Drain-to-Source On Resistance	$R_{DS(on)}$	N	$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}$		0.058	0.080	$\Omega$
		P	$V_{GS} = -4.5\text{ V}, I_D = -2.2\text{ A}$		0.130	0.155	
		N	$V_{GS} = 2.5\text{ V}, I_D = 2.3\text{ A}$		0.077	0.115	
		P	$V_{GS} = -2.5\text{ V}, I_D = -1.7\text{ A}$		0.200	0.240	
Forward Transconductance	$g_{FS}$	N	$V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		6.0		S
		P	$V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$		6.0		

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	N	$f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}$	180		pF		
		P		$V_{DS} = -10\text{ V}$	185				
Output Capacitance	$C_{OSS}$	N		$V_{DS} = 10\text{ V}$	80				
		P		$V_{DS} = -10\text{ V}$	95				
Reverse Transfer Capacitance	$C_{RSS}$	N		$V_{DS} = 10\text{ V}$	25				
		P		$V_{DS} = -10\text{ V}$	30				
Total Gate Charge	$Q_{G(TOT)}$	N		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		2.6		4.0	nC
		P		$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$		3.0		6.0	
Gate-to-Source Gate Charge	$Q_{GS}$	N	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		0.6				
		P	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$		0.5				
Gate-to-Drain "Miller" Charge	$Q_{GD}$	N	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		0.7				
		P	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.2\text{ A}$		0.9				

3. Pulse Test: Pulse Width  $\leq 250\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

# NTHC5513

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b> (Note 4)							
Turn-On Delay Time	t <sub>d(ON)</sub>	N	V <sub>DD</sub> = 16 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.9 A, R <sub>G</sub> = 2.5 Ω		5.0	10	ns
Rise Time	t <sub>r</sub>				9.0	18	
Turn-Off Delay Time	t <sub>d(OFF)</sub>				10	20	
Fall Time	t <sub>f</sub>				3.0	6.0	
Turn-On Delay Time	t <sub>d(ON)</sub>	P	V <sub>DD</sub> = -16 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -2.2 A, R <sub>G</sub> = 2.5 Ω		7.0	12	
Rise Time	t <sub>r</sub>				13	25	
Turn-Off Delay Time	t <sub>d(OFF)</sub>				33	50	
Fall Time	t <sub>f</sub>				27	40	

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage (Note 5)	V <sub>SD</sub>	N	V <sub>GS</sub> = 0 V	I <sub>S</sub> = 2.6 A		0.8	1.15	V
		P		I <sub>S</sub> = -2.1 A		-0.8	-1.15	
Reverse Recovery Time (Note 4)	t <sub>RR</sub>	N	V <sub>GS</sub> = 0 V, dI <sub>S</sub> / dt = 100 A/μs	I <sub>S</sub> = 1.5 A		12.5		ns
		P		I <sub>S</sub> = -1.5 A		32		
Charge Time	t <sub>a</sub>	N		I <sub>S</sub> = 1.5 A		9.0		
		P		I <sub>S</sub> = -1.5 A		10		
Discharge Time	t <sub>b</sub>	N		I <sub>S</sub> = 1.5 A		3.5		
		P		I <sub>S</sub> = -1.5 A		22		
Reverse Recovery Charge	Q <sub>RR</sub>	N		I <sub>S</sub> = 1.5 A		6.0		nC
		P		I <sub>S</sub> = -1.5 A		15		

4. Switching characteristics are independent of operating junction temperatures.  
 5. Pulse Test: Pulse Width ≤ 250 μs, Duty Cycle ≤ 2%.

TYPICAL N-CHANNEL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

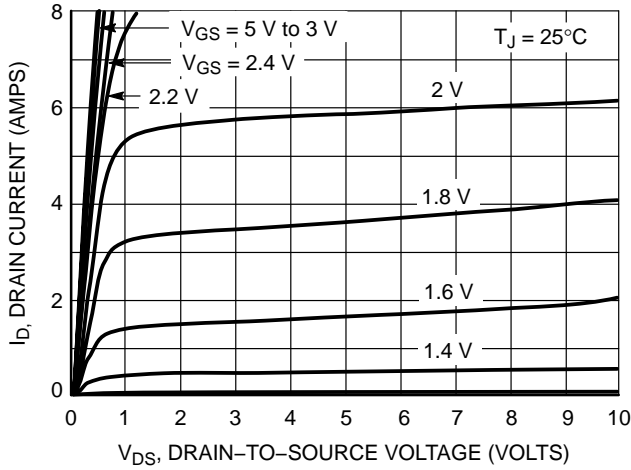


Figure 1. On-Region Characteristics

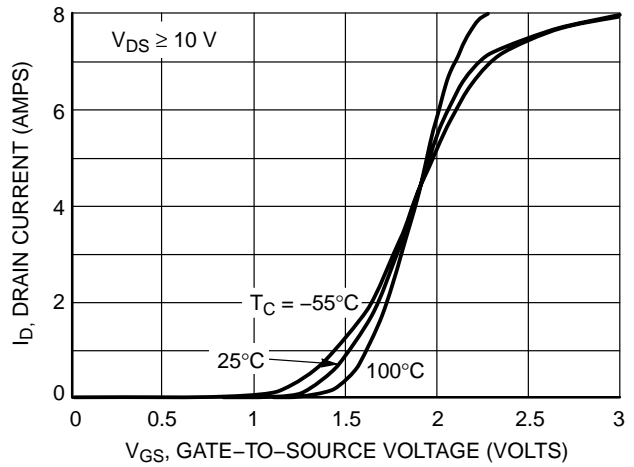


Figure 2. Transfer Characteristics

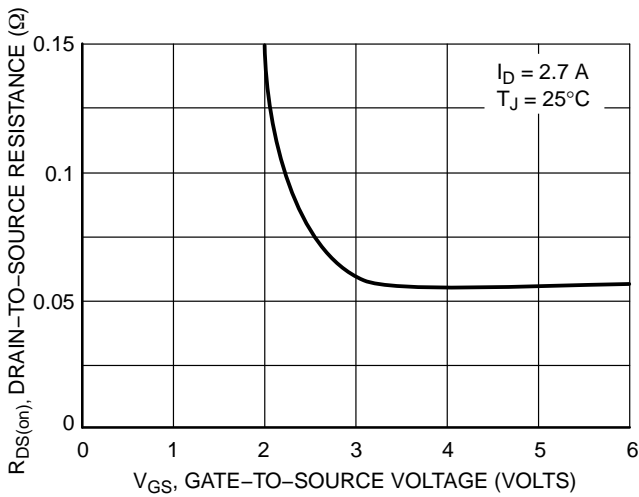


Figure 3. On-Resistance vs. Gate-to-Source Voltage

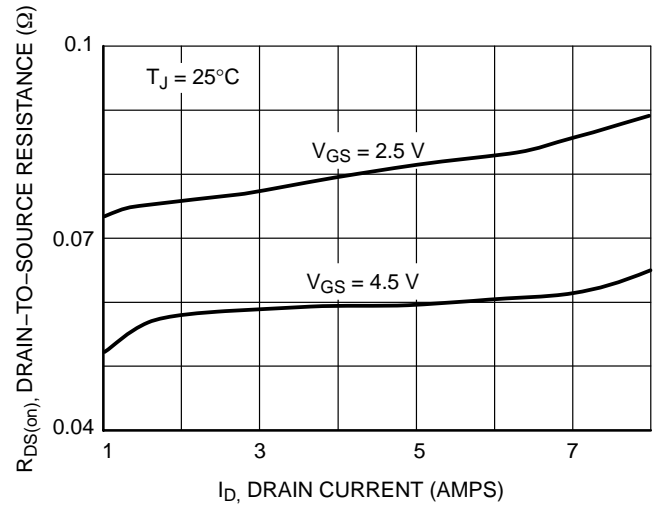


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

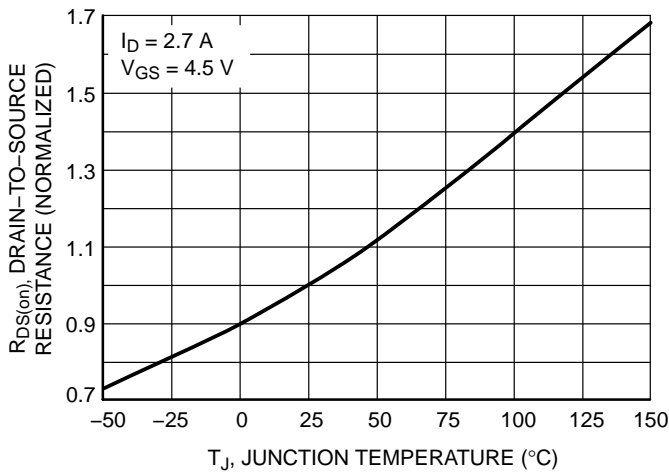


Figure 5. On-Resistance Variation with Temperature

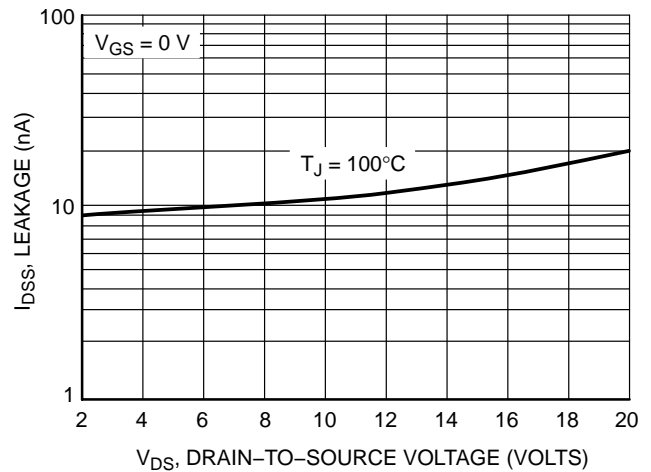


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL N-CHANNEL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

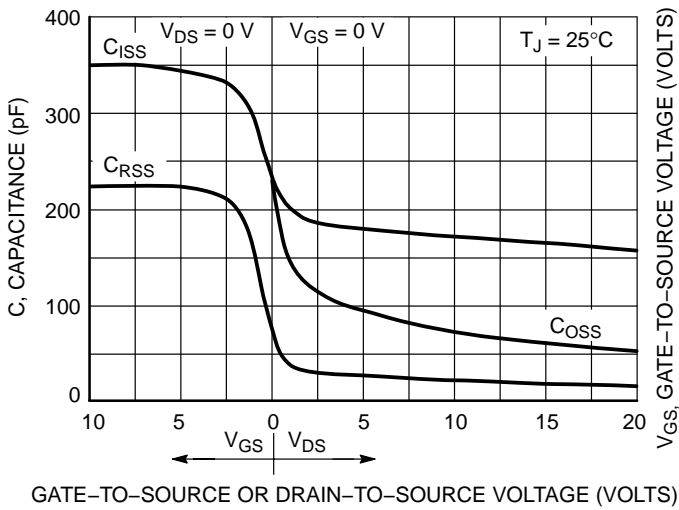


Figure 7. Capacitance Variation

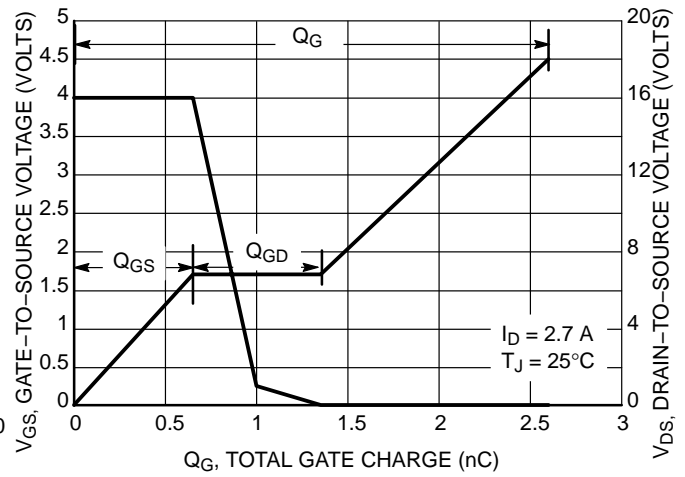


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

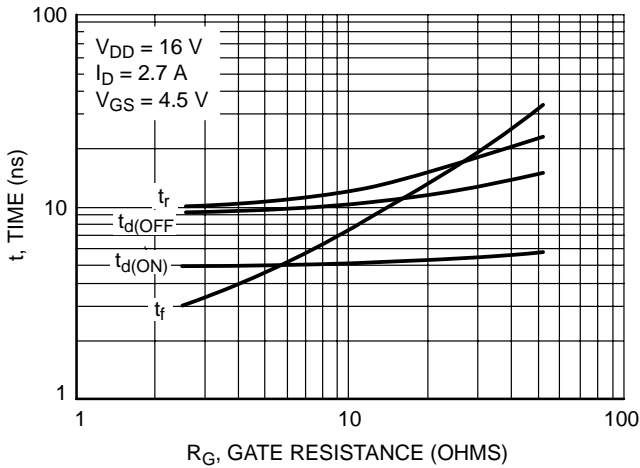


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

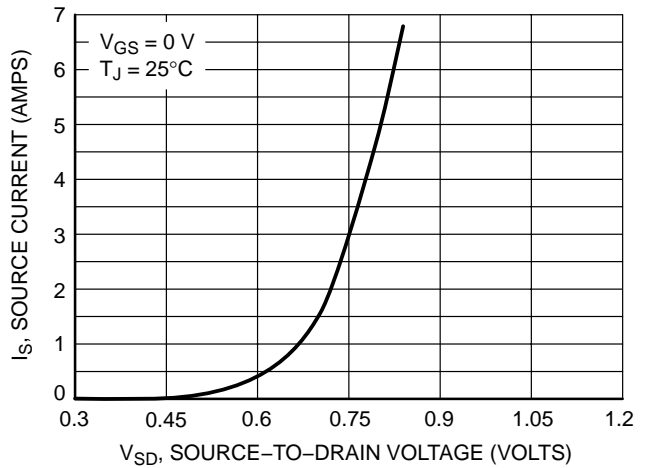


Figure 10. Diode Forward Voltage vs. Current

TYPICAL P-CHANNEL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

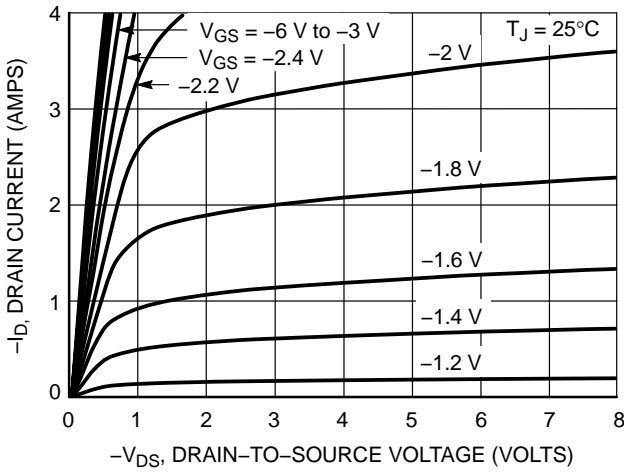


Figure 11. On-Region Characteristics

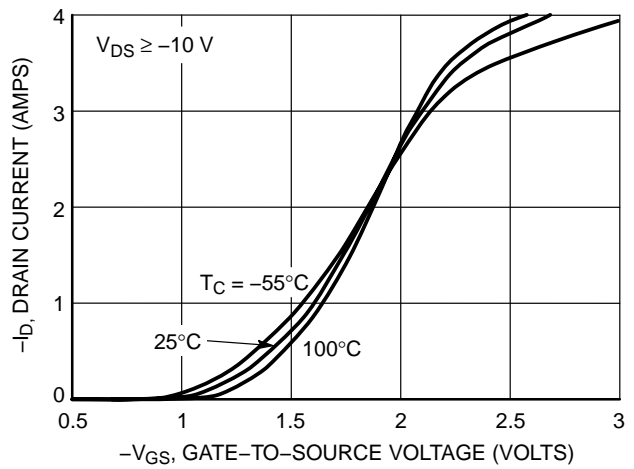


Figure 12. Transfer Characteristics

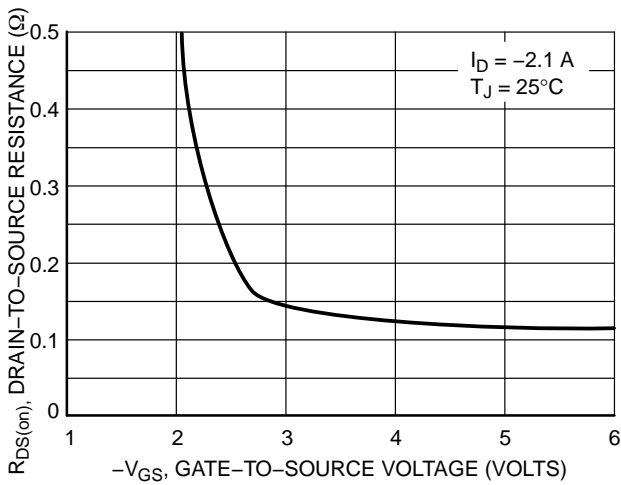


Figure 13. On-Resistance vs. Gate-to-Source Voltage

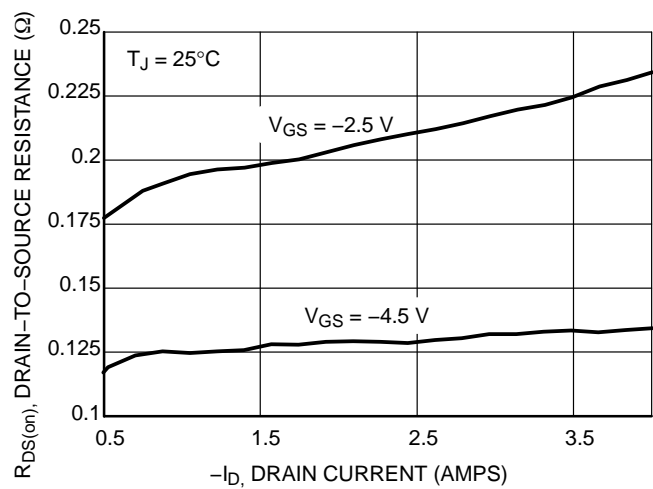


Figure 14. On-Resistance vs. Drain Current and Gate Voltage

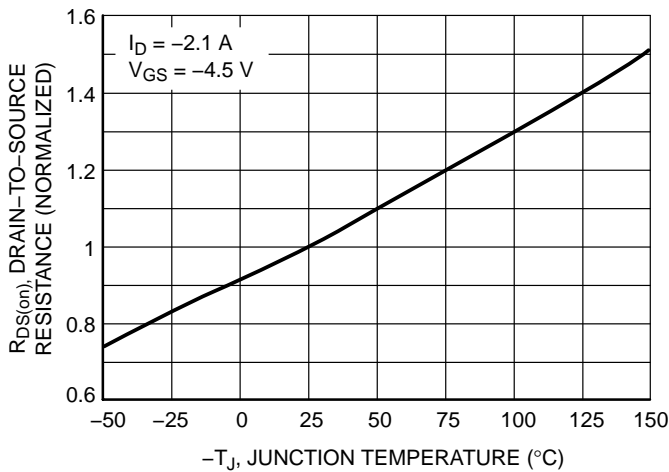


Figure 15. On-Resistance Variation with Temperature

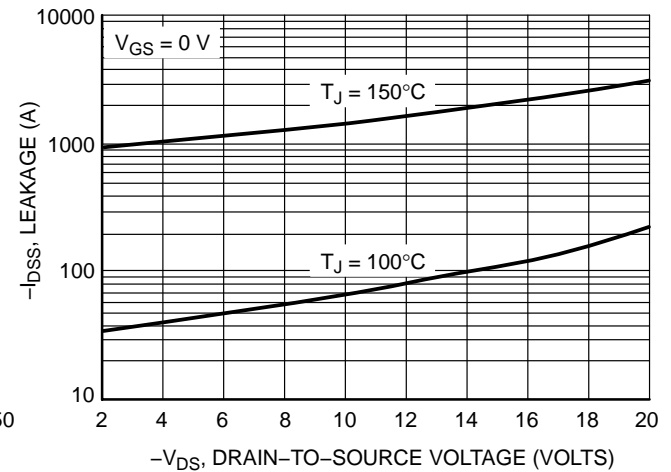


Figure 16. Drain-to-Source Leakage Current vs. Voltage

TYPICAL P-CHANNEL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

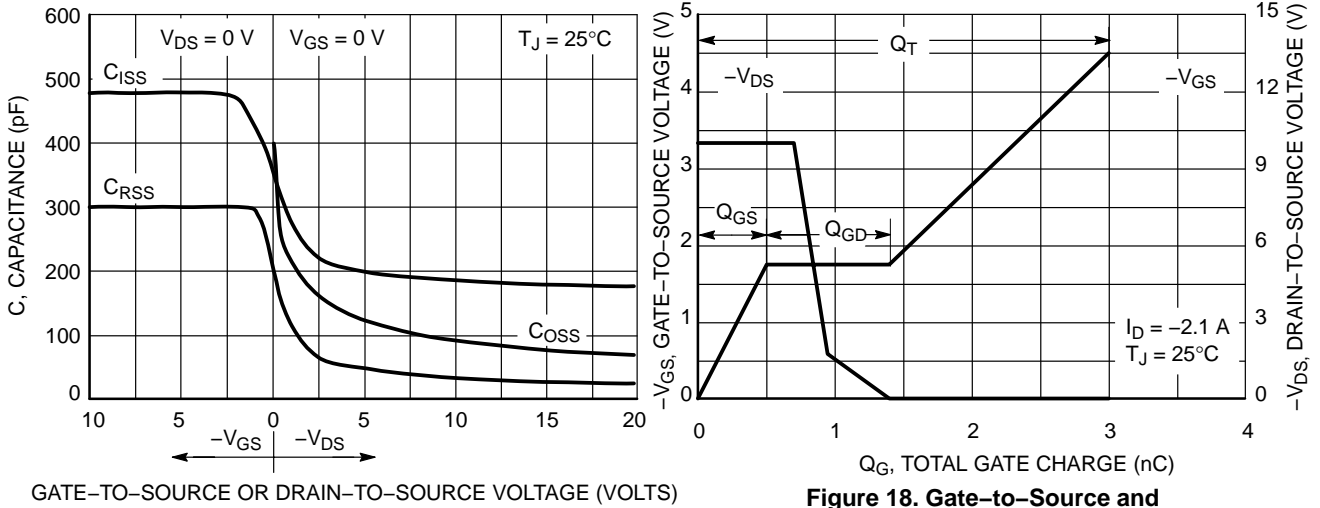


Figure 17. Capacitance Variation

Figure 18. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

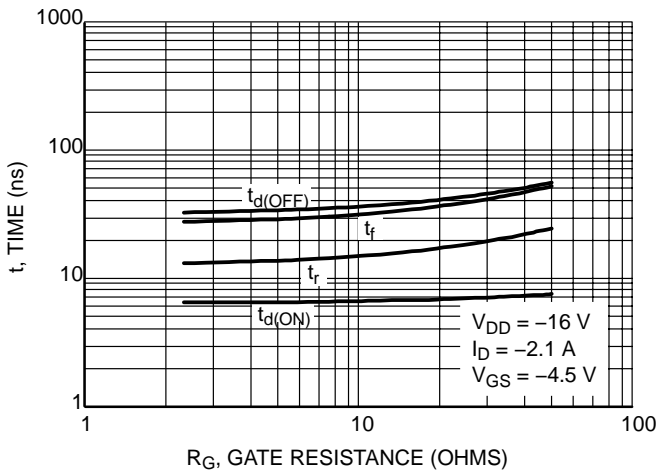


Figure 19. Resistive Switching Time Variation vs. Gate Resistance

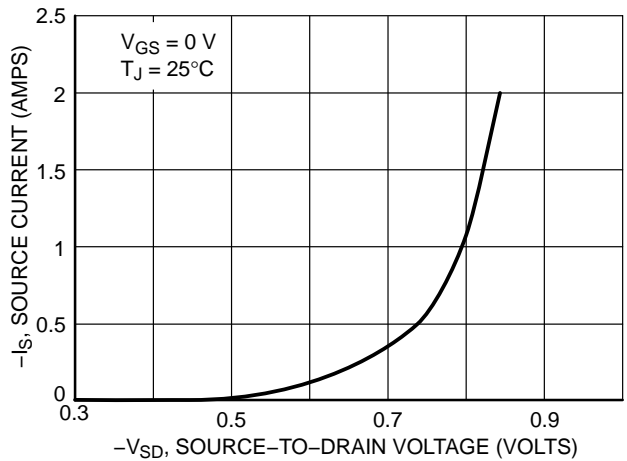


Figure 20. Diode Forward Voltage vs. Current

TYPICAL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

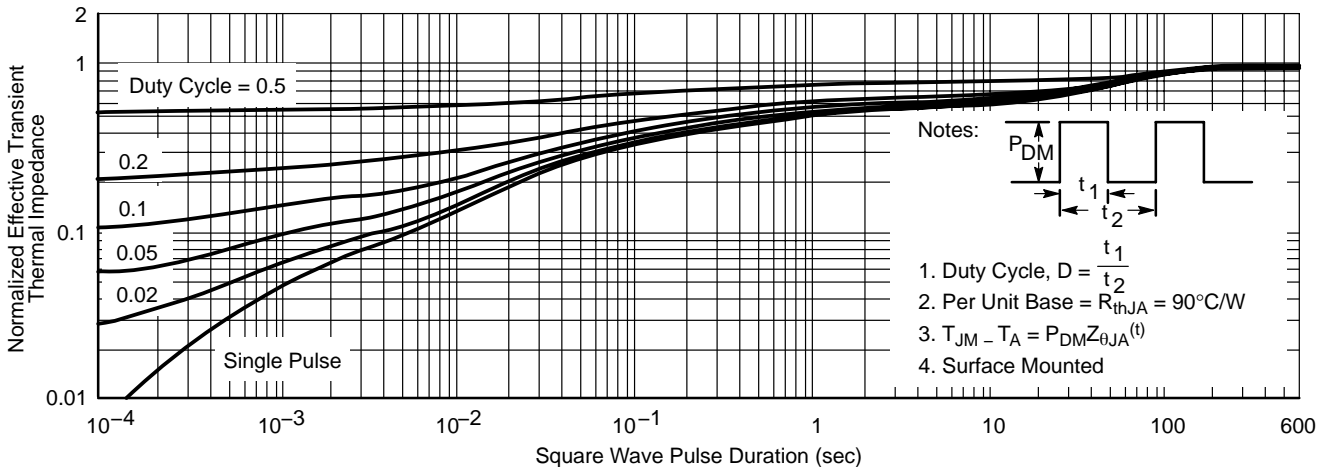


Figure 21. Thermal Response

# NTHC5513

## SOLDERING FOOTPRINT\*

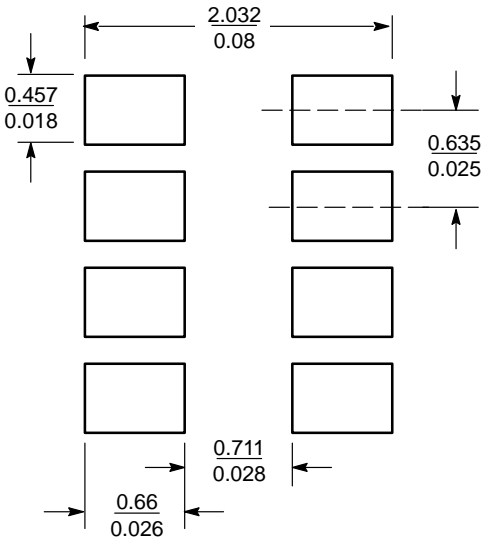


Figure 22. Basic

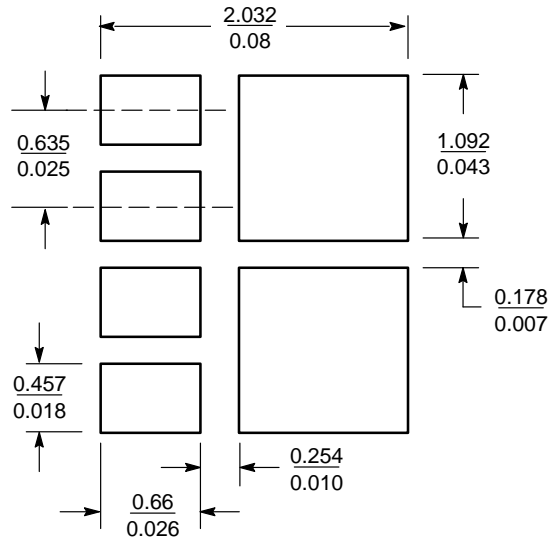


Figure 23. Style 2

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 22. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 23 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the

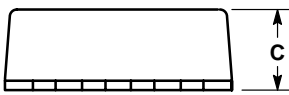
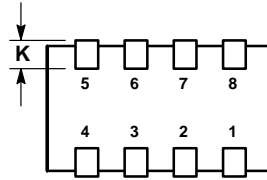
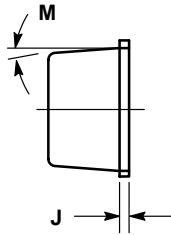
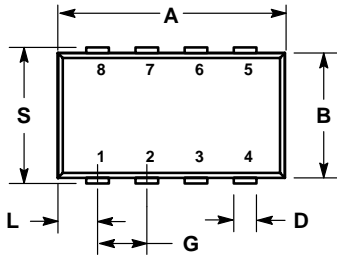
confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper lead-frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.



# NTHC5513

## PACKAGE DIMENSIONS

### ChipFET CASE 1206A-03 ISSUE E



$\Delta$  0.05 (0.002)


STYLE 2:  
PIN 1. SOURCE 1  
2. GATE 1  
3. SOURCE 2  
4. GATE 2  
5. DRAIN 2  
6. DRAIN 2  
7. DRAIN 1  
8. DRAIN 1

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5° NOM		5° NOM	
S	1.80	2.00	0.072	0.080

ChipFET is a trademark of Vishay Siliconix.

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your  
local Sales Representative.