19-3787; Rev 1; 9/06

EVALUATION KIT AVAILABLE

I²C Port Expander with 4 Push-Pull Outputs and 4 Inputs

General Description

The MAX7322 2-wire serial-interfaced peripheral features four push-pull outputs and four input ports with selectable internal pullups. Input ports are overvoltage protected to +6V and feature transition detection with interrupt output.

The four input ports are continuously monitored for state changes (transition detection). The interrupt is latched, allowing detection of transient changes. Any combination of inputs can be selected using the interrupt mask to assert the open-drain $\overline{INT}$ output. When the MAX7322 is subsequently accessed through the serial interface, any pending interrupt is cleared.

The four push-pull outputs are rated to sink 20mA, and are capable of driving LEDs.

The $\overline{RST}$ input clears the serial interface, terminating any I²C communication to or from the MAX7322.

The MAX7322 uses two address inputs with four-level logic to allow 16 I²C slave addresses. The slave address also sets the power-up default logic state for the four output ports, and enables or disables internal 40kΩ pullups for the input ports.

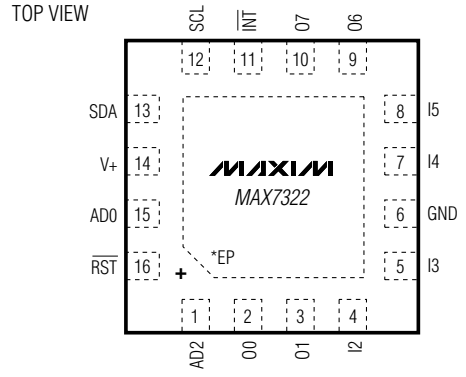
The MAX7322 is one device in a family of pin-compatible port expanders with a choice of input ports, open-drain I/O ports, and push-pull output ports (see Table 1).

The MAX7322 is available in 16-pin QSOP and TQFN packages, and is specified over the -40°C to +125°C automotive temperature range.

Applications

Cell Phones
SAN/NAS
Servers
Notebooks
Satellite Radio
Automotive

Pin Configurations



TQFN (3mm x 3mm)

Pin Configurations continued at end of data sheet.

Features

- **400kHz I²C Serial Interface**
- **+1.71V to +5.5V Operation Voltage**
- **4 Push-Pull Output Ports Rated at 20mA Sink Current**
- **4 Input Ports with Maskable, Latching Transition Detection**
- **Input Ports are Overvoltage Protected to +6V**
- **Transient Changes are Latched, Allowing Detection Between Read Operations**
- **$\overline{INT}$ Output Alerts Change on Any Selection of Inputs**
- **AD0 and AD2 Inputs Select from 16 Slave Addresses**
- **Low 0.6µA (typ) Standby Current**
- **-40°C to +125°C Operating Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	PKG CODE
MAX7322AEE+	-40°C to +125°C	16 QSOP	—	E16-4
MAX7322ATE+	-40°C to +125°C	16 TQFN-EP* (3mm x 3mm)	ADD	T1633-4

+Denotes lead-free package.

**EP = Exposed paddle.*

Selector Guide

PART	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS
MAX7319	8	Yes	—	—
MAX7320	—	—	—	8
MAX7321	Up to 8	—	Up to 8	—
MAX7322	4	Yes	—	4
MAX7323	Up to 4	—	Up to 4	4
MAX7328	Up to 8	—	Up to 8	—
MAX7329	Up to 8	—	Up to 8	—

Typical Application Circuit and Functional Diagram appear at end of data sheet.

I²C Port Expander with 4 Push-Pull Outputs and 4 Inputs

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
Supply Voltage V+.....-0.3V to +6V
SCL, SDA, AD0, AD2, $\overline{RST}$, $\overline{INT}$, I2–I5.....-0.3V to +6V
O0, O1, O6, O7.....-0.3 to V+ + 0.3V
O0, O1, O6, O7 Output Current.....±25mA
SDA Sink Current..... 10mA
$\overline{INT}$ Sink Current.....10mA
Total V+ Current.....50mA
Total GND Current 100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
16-Pin TQFN (derate 15.6mW/°C above +70°C) 1250mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		1.71		5.50	V
Power-On Reset Voltage	V_{POR}	V+ falling			1.6	V
Standby Current (Interface Idle)	I_{STB}	SCL and SDA and other digital inputs at V+		0.6	1.5	µA
Supply Current (Interface Running)	I_+	f_{SCL} = 400kHz; other digital inputs at V+		23	55	µA
Input High Voltage SDA, SCL, AD0, AD2, $\overline{RST}$, I2–I5	V_{IH}	V+ < 1.8V	0.8 x V+			V
		V+ ≥ 1.8V	0.7 x V+			
Input Low Voltage SDA, SCL, AD0, AD2, $\overline{RST}$, I2–I5	V_{IL}	V+ < 1.8V			0.2 x V+	V
		V+ ≥ 1.8V			0.3 x V+	
Input Leakage Current SDA, SCL, AD0, AD2, $\overline{RST}$, I2–I5	I_{IH}, I_{IL}	SDA, SCL, AD0, AD2, $\overline{RST}$, at V+ or GND, internal pullup disabled	-0.2		+0.2	µA
Input Capacitance SDA, SCL, AD0, AD2, $\overline{RST}$, I2–I5				10		pF
Output Low Voltage O0, O1, O6, O7	V_{OL}	V+ = +1.71V, I_{SINK} = 5mA		90	180	mV
		V+ = +2.5V, I_{SINK} = 10mA		110	210	
		V+ = +3.3V, I_{SINK} = 15mA		130	230	
		V+ = +5V, I_{SINK} = 20mA		140	250	
Output High Voltage O0, O1, O6, O7	V_{OH}	V+ = +1.71V, I_{SOURCE} = 2mA	V+ - 250	V+ - 30		mV
		V+ = +2.5V, I_{SOURCE} = 5mA	V+ - 360	V+ - 70		
		V+ = +3.3V, I_{SOURCE} = 5mA	V+ - 260	V+ - 100		
		V+ = +5V, I_{SOURCE} = 10mA	V+ - 360	V+ - 120		
Output Low Voltage SDA	V_{OLSDA}	I_{SINK} = 6mA			250	mV
Output Low Voltage $\overline{INT}$	V_{OLINT}	I_{SINK} = 5mA		130	250	mV
Port Input Pullup Resistor	R_{PU}		25	40	55	kΩ

PORT AND INTERRUPT $\overline{INT}$ TIMING CHARACTERISTICS

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Output Data Valid	t_{PPV}	$C_L \le 100pF$			4	µs
Port Input Setup Time	t_{PSU}	$C_L \le 100pF$	0			µs
Port Input Hold Time	t_{PH}	$C_L \le 100pF$	4			µs
$\overline{INT}$ Input Data Valid Time	t_{IV}	$C_L \le 100pF$			4	µs
$\overline{INT}$ Reset Delay Time from STOP	t_{IP}	$C_L \le 100pF$			4	µs
$\overline{INT}$ Reset Delay Time from Acknowledge	t_{IR}	$C_L \le 100pF$			4	µs

TIMING CHARACTERISTICS

(V+ = +1.71V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 2)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 3, 4)		$20 + 0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 3, 4)		$20 + 0.1C_b$	300	ns
Fall Time of SDA, Transmitting	$t_{F,TX}$	(Notes 3, 4)		$20 + 0.1C_b$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 5)		50		ns
Capacitive Load for Each Bus Line	C_b	(Note 3)			400	pF
$\overline{RST}$ Pulse Width	t_W		500			ns
$\overline{RST}$ Rising to START Condition Setup Time	$t_{\overline{RST}}$		1			µs

Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

Note 3: Guaranteed by design.

Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 x V+ and 0.7 x V+ with $I_{SINK} \le 6mA$.

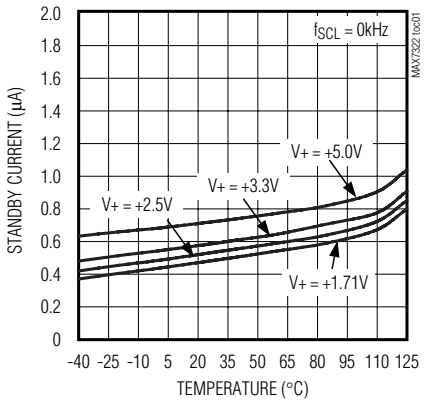
Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

I²C Port Expander with 4 Push-Pull Outputs and 4 Inputs

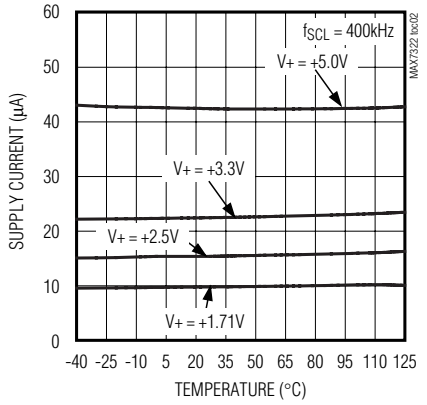
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

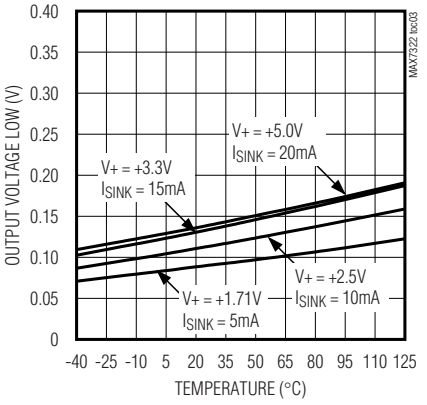
STANDBY CURRENT vs. TEMPERATURE



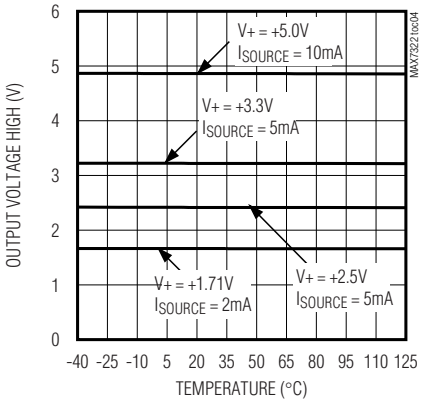
SUPPLY CURRENT vs. TEMPERATURE



OUTPUT VOLTAGE LOW vs. TEMPERATURE



OUTPUT VOLTAGE HIGH vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1, 3	15, 1	AD0, AD2	Address Inputs. Select device slave address with AD0 and AD2. Connect AD0 and AD2 to either GND, V+, SCL, or SDA to give four logic combinations (see Table 2).
2	16	$\overline{RST}$	Reset Input. Active Low. Drive $\overline{RST}$ low to clear the 2-wire interface.
4, 5, 11, 12,	2, 3, 9, 10	O0, O1, O6, O7	Push-Pull Output Ports
6, 7, 9, 10	4, 5, 7, 8	I2–I5	Input Ports. I2 to I5 are CMOS-logic inputs protected to +6V.
8	6	GND	Ground
13	11	$\overline{INT}$	Interrupt Output, Active Low. $\overline{INT}$ is an open-drain output.
14	12	SCL	I²C-Compatible Serial Clock Input
15	13	SDA	I²C-Compatible Serial Data I/O
16	14	V+	Positive Supply Voltage. Bypass V+ to GND with a ceramic capacitor of at least 0.047µF.
—	EP	EP	Exposed Paddle. Connect exposed pad to GND.

Detailed Description

MAX7319–MAX7329 Family Comparison

The MAX7319–MAX7323 family consists of five pin-compatible, eight-port expanders. Each version is optimized for different applications. The MAX7328 and MAX7329 are industry-standard parts.

The MAX7324–MAX7327 family consists of four pin-compatible, 16-port expanders that integrate the functions of the MAX7320 and one of either MAX7319, MAX7321, MAX7322, or MAX7323.

Functional Overview

The MAX7322 is a general-purpose port expander operating from +1.71V to +5.5V supply that provides four push-pull output ports with 20mA sink, 10mA source drive capability, and four input ports that are overvoltage protected to +6V independent of supply voltage. The MAX7322 is rated to sink a total of 100mA and source a total of 50mA from all four combined outputs.

The MAX7322 is set to one of 16 I²C slave addresses (0x60 to 0x6F) using address inputs AD2 and AD0, and is accessed over an I²C serial interface up to 400kHz. The $\overline{RST}$ input clears the serial interface in case of a bus lockup, terminating any serial transaction to or from the MAX7322.

Table 1. MAX7319–MAX7329 Family Comparison

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	I²C DATA WRITE	I²C DATA READ	APPLICATION
8-PORT EXPANDERS								
MAX7319	110xxxx	8	Yes	—	—	<I7–I0 interrupt mask>	<I7–I0 port inputs> <I7–I0 transition flags>	Input-only versions: 8 input ports with programmable latching transition detection interrupt and selectable pullups. Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7320	101xxxx	—	—	—	8	<O7–O0 port outputs>	<O7-O0 port inputs>	Output-only versions: 8 push-pull outputs with selectable power-up default levels. Push-pull outputs offer faster rise time than open-drain outputs, and require no pullup resistors.

I2C Port Expander with 4 Push-Pull Outputs and 4 Inputs

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	I²C DATA WRITE	I²C DATA READ	APPLICATION
MAX7321	110xxxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs> <P7–P0 transition flags>	I/O versions: 8 open-drain I/O ports with latching transition detection interrupt and selectable pullups. Open-drain outputs can level shift the logic-high state to a higher or lower voltage than V+ using external pullup resistors. Any port can be used as an input by setting the open-drain output to logic-high. Transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7322	110xxxx	4	Yes	—	4	<O7, O6 outputs, I5–I2 interrupt mask, O1, O0 outputs>	<O7, O6, I5–I2, O1, O0 port inputs> <0, 0, I5–I2 transition flags, 0, 0>	4 input-only, 4 output-only versions: 4 input ports with programmable latching transition detection interrupt and selectable pullups; 4 push-pull outputs with selectable power-up default levels.
MAX7323	110xxxx	Up to 4	—	Up to 4	4	<port outputs>	<O7, O6, P5–P2, O1, O0 port inputs> <0, 0, P5–P2 transition flags, 0, 0>	4 I/O, 4 output-only versions: 4 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 4 push-pull outputs with selectable power-up default levels.
MAX7328 MAX7329	0100xxx 0111xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>	8 open-drain I/O ports with nonlatching transition detection interrupt and pullups on all ports. All ports power up as inputs (or logic-high outputs). Any port can be used as an input by setting the open-drain output to logic-high.

Table 1. MAX7319–MAX7329 Family Comparison (continued)

PART	I²C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	I²C DATA WRITE	I²C DATA READ	APPLICATION
16-PORT EXPANDERS								
MAX7324	101xxxx and 110xxxx	8	Yes	—	8	—	—	Software equivalent to a MAX7320 plus a MAX7319.
MAX7325		Up to 8	—	Up to 8	8	—	—	Software equivalent to a MAX7320 plus a MAX7321.
MAX7326		4	Yes	—	12	—	—	Software equivalent to a MAX7320 plus a MAX7322.
MAX7327		Up to 4	—	Up to 4	12	—	—	Software equivalent to a MAX7320 plus a MAX7323.

When the MAX7322 is read through the serial interface the actual logic levels at the ports are read back.

The four input ports offer latching transition detection functionality. All input ports are continuously monitored for changes. An input change sets 1 of 4 flag bits that identify the changed input(s). All flags are cleared upon a subsequent read or write transaction to the MAX7322.

A latching interrupt output, $\overline{INT}$, is programmed to flag input data changes on the four input ports through an interrupt mask register. By default, data changes on any input port force $\overline{INT}$ to a logic low. The interrupt output $\overline{INT}$ and all transition flags are deasserted when the MAX7322 is next accessed through the serial interface.

Internal pullup resistors to V+ are selected by the address select inputs, AD0 and AD2. Pullups are enabled on the input ports in groups of two (see Table 2).

Output port power-up logic states are selected by the address select inputs AD0 and AD2. Ports default to logic-high or logic-low on power-up in groups of two (see Table 2).

Initial Power-Up

On power-up, the transition detection logic is reset, and $\overline{INT}$ is deasserted. The interrupt mask register is set to 0x3C, enabling the interrupt output for transitions on all four input ports. The transition flags are cleared to indicate no data changes. The power-up default state of the four push-pull outputs are set according to the I²C slave address selection inputs, AD0 and AD2 (Table 2).

Power-On Reset (POR)

The MAX7322 contains an integral POR circuit that ensures all registers are reset to a known state on power-up. When V+ rises above V_{POR} (1.6V max), the POR circuit releases the registers and 2-wire interface for normal operation. When V+ drops to less than V_{POR}, the MAX7322 resets all register contents to the POR defaults (Table 2).

$\overline{RST}$ Input

The active-low $\overline{RST}$ input operates as a reset that voids any current I²C transaction involving the MAX7322, forcing the MAX7322 into the I²C STOP condition. The reset action does not clear the interrupt output ($\overline{INT}$).

Standby Mode

When the serial interface is idle, the MAX7322 automatically enters standby mode, drawing minimal supply current.

Slave Address and Input Pullup Selection/Default Logic State

Address inputs AD0 and AD2 determine the MAX7322 slave address, select which inputs have pullup resistors and set the default logic state for outputs. Pullups are enabled on the input ports in groups of two (see Table 2). The MAX7319, MAX7321, MAX7322, and MAX7323 use a different range of slave addresses (110xxxx) than the MAX7320 (101xxxx).

The MAX7322 slave address is determined on each I²C transmission, regardless of whether the transmission is actually addressing the MAX7322. The MAX7322 distinguishes whether address inputs AD2 and AD0 are connected to SDA or SCL instead of fixed logic levels V+ or GND during this transmission. This means that the MAX7322 slave address can be configured dynamically in the application without cycling the device supply.

I²C Port Expander with 4 Push-Pull Outputs and 4 Inputs

On initial power-up, the MAX7322 cannot decode the address inputs AD2 and AD0 fully until the first I²C transmission. AD0 and AD2 initially appear to be connected to V+ or GND. This is important because the address selection determines the power-up logic state, and whether pullups are enabled. However, at power-up, the I²C SDA and SCL bus interface lines are high impedance at the pins of every device (master or slave) connected to the bus, including the MAX7322. This is guaranteed as part of the I²C specification. Therefore, address inputs AD2 and AD0 that are connected to SDA or SCL normally appear at power-up to be connected to V+. The port selection logic uses AD0 to select whether pullups are enabled for ports I2 and I3, and to set the initial logic state for ports O0 and O1. AD2 selects whether pullups are enabled for ports I4 and I5 and sets the internal logic state for ports O6 and O7. The rule is that a logic-high, SDA, or SCL connection selects the pullups and sets the default logic state high. A logic-low deselects the pullups and sets the default logic state low (Table 2). This means that the port configuration is correct on power-up for a standard I²C configuration, where SDA or SCL are pulled up to V+ by the external I²C pullup resistors.

There are circumstances where the assumption that SDA = SCL = V+ on power-up is not true—for example, in applications in which there is legitimate bus activity during power-up. Also, if SDA and SCL are terminated with pullup resistors to a different supply voltage than the MAX7322's supply voltage, and if that pullup supply rises later than the MAX7322's supply, then SDA or SCL may appear at power-up to be connected to GND. In such applications, use the four address combinations that are selected by connecting address inputs AD2 and AD0 to V+ or GND (shown in **bold** in Table 2). These selections are guaranteed to be correct at power-up, independent of SDA and SCL behavior. If one of the other 12 address combinations is used, an unexpected combination of pullups might be asserted until the first I²C transmission (to any device, not necessarily the MAX7322) is put on the bus, and an unexpected combination of ports may initialize as logic-low outputs instead of inputs or logic-high outputs.

Port Inputs

Port inputs switch at CMOS logic levels as determined by the expander's supply voltage, and are overvoltage tolerant to +6V, independent of the expander's supply voltage.

Port Input Transition Detection

All four input ports are monitored for changes since the expander was last accessed through the serial interface. The state of the I/O ports is stored in an internal

Table 2. MAX7322 Address Map

PIN CONNECTION		DEVICE ADDRESS							OUTPUTS POWER—UP DEFAULT								40kΩ INPUT PULLUPS ENABLED							
AD2	**AD0**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**O7**	**O6**	**I5**	**I4**	**I3**	**I2**	**O1**	**O0**	**O7**	**O6**	**I5**	**I4**	**I3**	**I2**	**O1**	**O0**
SCL	GND	1	1	0	0	0	0	0	1	1	Inputs				0	0	Pullups are not enabled for push-pull outputs		Y	Y	—	—	Pullups are not enabled for push-pull outputs	
SCL	V+	1	1	0	0	0	0	1	1	1					1	1			Y	Y	Y	Y		
SCL	SCL	1	1	0	0	0	1	0	1	1					1	1			Y	Y	Y	Y		
SCL	SDA	1	1	0	0	0	1	1	1	1					1	1			Y	Y	Y	Y		
SDA	GND	1	1	0	0	1	0	0	1	1					0	0			Y	Y	—	—		
SDA	V+	1	1	0	0	1	0	1	1	1					1	1			Y	Y	Y	Y		
SDA	SCL	1	1	0	0	1	1	0	1	1					1	1			Y	Y	Y	Y		
SDA	SDA	1	1	0	0	1	1	1	1	1					1	1			Y	Y	Y	Y		
GND	**GND**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**					**0**	**0**			**—**	**—**	**—**	**—**		
GND	**V+**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**					**1**	**1**			**—**	**—**	**Y**	**Y**		
GND	SCL	1	1	0	1	0	1	0	0	0					1	1			—	—	Y	Y		
GND	SDA	1	1	0	1	0	1	1	0	0					1	1			—	—	Y	Y		
V+	**GND**	**1**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**1**					**0**	**0**			**Y**	**Y**	**—**	**—**		
V+	**V+**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**1**					**1**	**1**			**Y**	**Y**	**Y**	**Y**		
V+	SCL	1	1	0	1	1	1	0	1	1					1	1			Y	Y	Y	Y		
V+	SDA	1	1	0	1	1	1	1	1	1					1	1			Y	Y	Y	Y		

"snapshot" register for transition monitoring. The snapshot is continuously compared with the actual input conditions, and if a change is detected for any port input, then an internal transition flag is set for that port, and $\overline{INT}$ is asserted to signal a state change. The four port inputs are sampled (internally latched into the snapshot register) and the old transition flags cleared during the I²C acknowledge of every MAX7322 read and write access. The previous port transition flags are read through the serial interface as the second byte of a 2-byte read sequence.

A long read sequence (more than 2 bytes) can be used to poll the expander continuously without the overhead of resending the slave address. If more than 2 bytes are read from the expander, the expander repeatedly returns the input port data alternating with the transition flags. The inputs are repeatedly resampled and the transition flags repeatedly reset for each pair of bytes read. All changes that occur during a long read sequence are detected and reported.

The MAX7322 includes a 4-bit interrupt mask register that selects which inputs generate an interrupt upon change. Each input's transition flag is set when its input changes, independent of the interrupt mask register settings. The interrupt mask register allows the processor to be interrupted for critical events, while the inputs and the transition flags can be polled periodically to detect less-critical events.

The $\overline{INT}$ output is not reasserted during a read sequence to avoid recursive reentry into an interrupt service routine. Instead, if a data change occurs that would normally cause the $\overline{INT}$ output to be set, the $\overline{INT}$ assertion is delayed until the STOP condition. $\overline{INT}$ is not reasserted upon a STOP condition if the changed input data is read before the STOP occurs. The $\overline{INT}$ logic ensures that unnecessary interrupts are not asserted, yet data changes are detected and reported no matter when the change occurs.

Transition Detection Masks

The transition detection logic incorporates a change flag and an interrupt mask bit for each of the four input ports. The four change flags can be read through the serial interface, and the 4-bit interrupt mask is set through the serial interface.

Each port's change flag is set when that port's input changes, and the change flag remains set even if the input returns to its original state. The port's interrupt mask determines whether a change on that input port generates an interrupt. Enable interrupts for high-priority inputs using the interrupt mask. The interrupt allows the system to respond quickly to changes on these inputs. Poll the MAX7322 periodically to monitor less-important inputs. The change flags indicate whether a permanent or transient change has occurred on any input since the MAX7322 was last accessed.

Port Outputs

Write one byte to the MAX7322 to set the output port levels for the four push-pull outputs, and the interrupt mask for the four inputs simultaneously.

Serial Interface

Serial Addressing

The MAX7322 operates as a slave that sends and receives data through an I²C interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). The master initiates all data transfers to and from the MAX7322 and generates the SCL clock that synchronizes the data transfer (Figure 1).

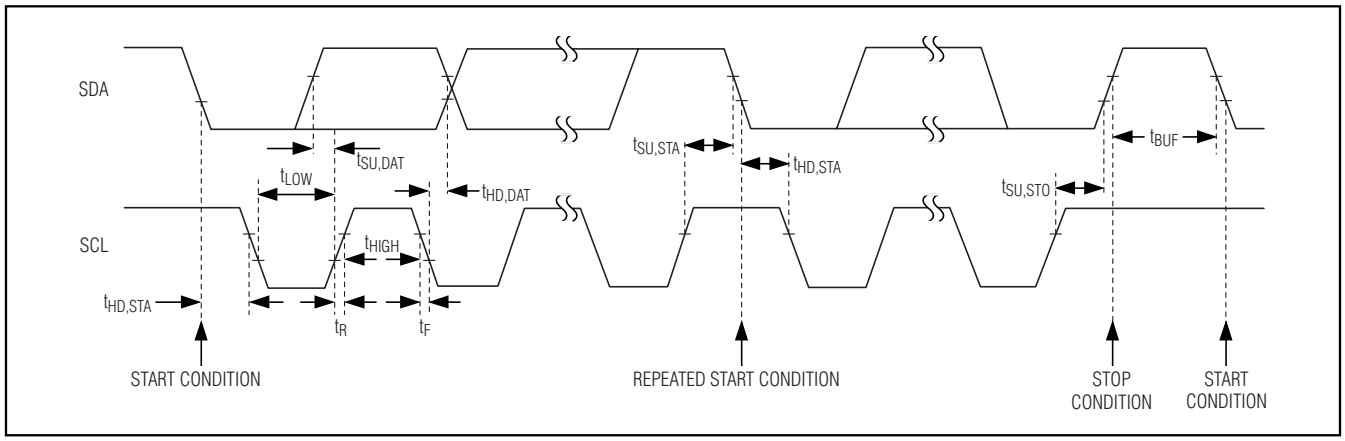


Figure 1. 2-Wire Serial Interface Timing Details

I²C Port Expander with 4 Push-Pull Outputs and 4 Inputs

SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition sent by a master, followed by the MAX7322's 7-bit slave address plus R/$\overline{W}$ bit, one or more data bytes, and finally a STOP condition (Figure 2).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 2).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 3).

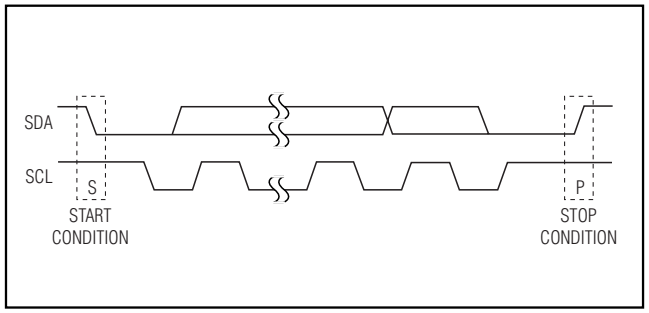


Figure 2. START and STOP Conditions

Acknowledge

The acknowledge bit is a clocked 9th bit the recipient uses to acknowledge receipt of each byte of data (Figure 4). Each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7322, the MAX7322 generates the acknowledge bit because the device is the recipient. When the MAX7322 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

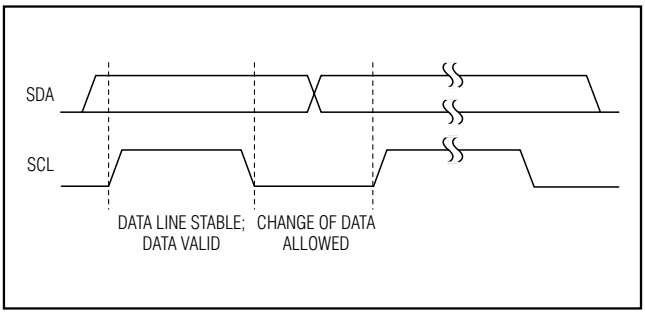


Figure 3. Bit Transfer

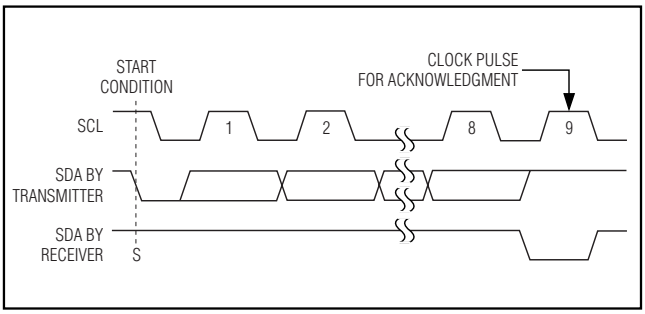


Figure 4. Acknowledge

Slave Address

The MAX7322 has a 7-bit-long slave address (Figure 5). The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command, and high for a read command.

The first (A6), second (A5), and third (A4) bits of the MAX7322 slave address are always 1, 1, and 0. Connect AD2 and AD0 to GND, V+, SDA, or SCL to select slave address bits A3, A2, A1, and A0. The MAX7322 has 16 possible slave addresses (Table 2), allowing up to 16 MAX7322 devices on an I²C bus.

Accessing the MAX7322

The MAX7322 is accessed through an I²C interface. The transition flags are cleared, and $\overline{INT}$ is deasserted each time the device acknowledges the I²C slave address.

A **single-byte read** from the MAX7322 returns the status of the four input ports and the four output ports (read back as inputs).

A **2-byte read** returns the status of the four input ports and the four output ports (as for a single-byte read), followed by the transition flags for the four input ports.

A **multibyte read** (more than 2 bytes before the I²C STOP bit) repeatedly returns the port data, alternating with the transition flags. As the data is resampled for each transmission, and the transition flags are reset each time, a multibyte read continuously returns the current data and identifies any changing ports.

If a port data change occurs during the read sequence, $\overline{INT}$ is reasserted after the I²C STOP bit. The MAX7322 does not generate another interrupt during a single-byte or multibyte read.

Port data is sampled during the preceding I²C acknowledge bit (the acknowledge bit for the I²C slave address in the case of a single-byte or 2-byte read).

A **single-byte write** to the MAX7322 sets the logic state of the four output ports and the 4-bit interrupt mask resistor, and clears both the internal transition flags and the $\overline{INT}$ output when the device acknowledges the slave address byte.

A **multibyte write** to the MAX7322 repeatedly sets the logic state of the four output ports and the 4-bit interrupt mask register.

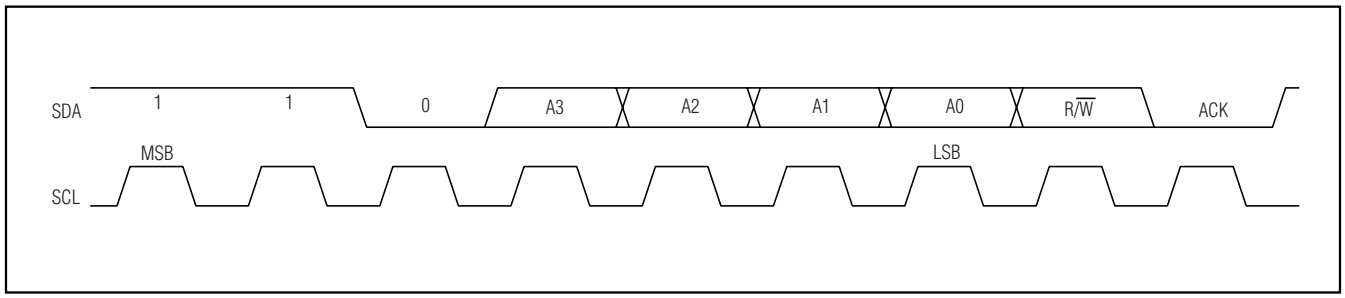


Figure 5. Slave Address

I²C Port Expander with 4 Push-Pull Outputs and 4 Inputs

Reading from the MAX7322

A read from the MAX7322 starts with the master transmitting the MAX7322's slave address with the R/$\overline{W}$ bit set high. The MAX7322 acknowledges the slave address, and samples the ports during the acknowledge bit. $\overline{INT}$ deasserts during the slave address acknowledge.

Typically, the master reads one or two bytes from the MAX7322, each byte being acknowledged by the master upon reception with the exception of the last byte.

When the master reads one byte from the MAX7322 and subsequently issues a STOP condition (Figure 6), the MAX7322 transmits the current port data, clears the change flags, and restarts the transition detection. $\overline{INT}$ deasserts during the slave address acknowledge. The new snapshot data is the current input port data transmitted to the master, so any input port changes that occur during the transmission are detected. $\overline{INT}$ remains high until the STOP condition.

The master can read two bytes from the MAX7322 and then issue a STOP condition (Figure 7). In this case, the MAX7322 transmits the current port data, followed by the change flags. The change flags are then cleared, and transition detection restarts. $\overline{INT}$ deasserts during the slave address acknowledge. The new snapshot

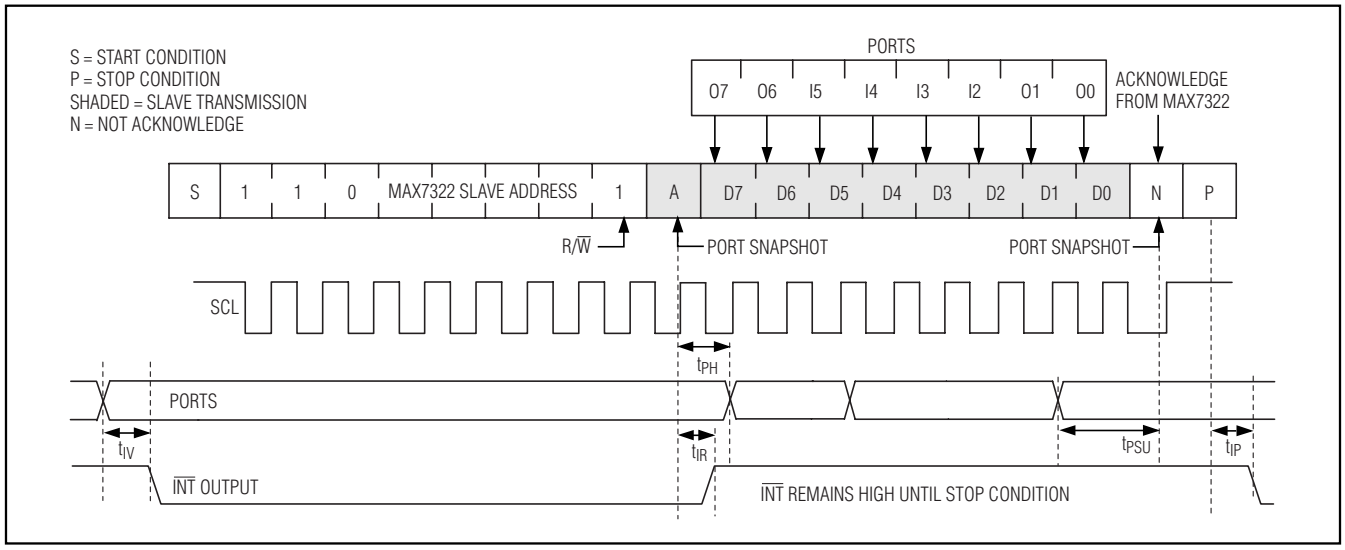


Figure 6. Reading from the MAX7322 (1 Data Byte)

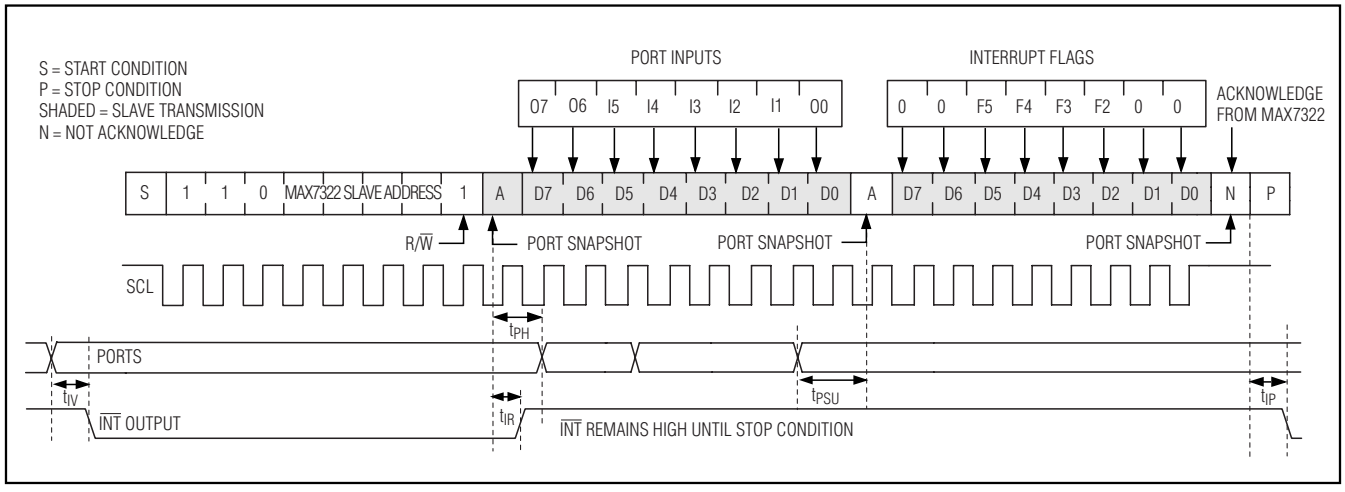


Figure 7. Reading from the MAX7322 (2 Data Bytes)

data is the current port data transmitted to the master, so any input port changes occurring during the transmission are detected. $\overline{INT}$ remains high until the STOP condition.

Writing to the MAX7322

A write to the MAX7322 starts with the master transmitting the MAX7322's slave address with the R/$\overline{W}$ bit set low. The MAX7322 acknowledges the slave address, and samples the ports (takes a snapshot) during acknowledge. $\overline{INT}$ deasserts during the slave acknowledge. The master proceeds to transmit 1 or more bytes of data. The MAX7322 acknowledges these subsequent bytes of data and updates the four output ports and the 4-bit interrupt mask register with each new byte until the master issues a STOP condition (Figure 8).

Applications Information

Port Input and I²C Interface Level Translation from Higher or Lower Logic Voltages

The MAX7322's SDA, SCL, AD0, AD2, input $\overline{RST}$, $\overline{INT}$, and input ports I2–I5 are overvoltage protected to +6V independent of V+. This allows the MAX7322 to operate from a lower supply voltage, such as +3.3V, while the I²C interface and/or some of the four input ports are driven from a higher logic level, such as +5V.

The MAX7322 can operate from a higher supply voltage, such as +3V, while the I²C interface and/or some of the four input ports I2–I5 are driven from a lower logic level, such as +2.5V. Apply a minimum voltage of 0.7 x V+ to assert a logic-high on any input. For example, a MAX7322 operating from a +5V supply may not recognize a +3.3V nominal logic-high. One solution for input-level translation is to drive the MAX7322 inputs from open-drain outputs. Use a pullup resistor to V+ or a higher supply to ensure a high logic voltage of greater than 0.7 x V+.

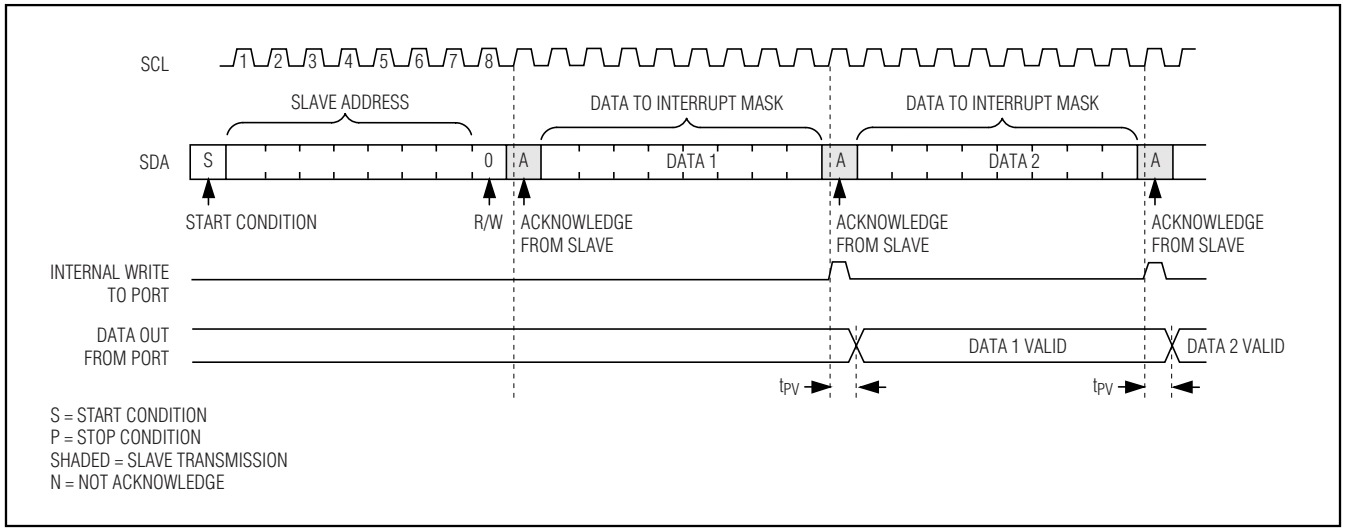


Figure 8. Writing to the MAX7322

I2C Port Expander with 4 Push-Pull Outputs and 4 Inputs

Port Structures

Each of the four output ports O0, O1, O6, and O7 has protection diodes to V+ and to GND (Figure 9). When a port output is driven to a voltage lower than GND, the appropriate protection diode clamps the output to a diode drop above V+ or below GND. When the MAX7322 is powered down (V+ = 0), each output port appears as a diode clamp to GND (Figure 9).

Each of the four input ports I2–I5 has a protection diode to GND (Figure 10). When a port input is driven to a voltage lower than GND, the protection diode will clamp the input to a diode drop below GND.

Each of the four inputs ports I2–I5 also has a 40kΩ (typ) pullup resistor that can be enabled or disabled. When a port is driven to a voltage higher than V+, the body diode of the pullup enable switch conducts and the 40kΩ pullup resistor is enabled. When the MAX7322 is powered down (V+ = 0), each input port appears as a 40kΩ pullup resistor in series with a diode connected to zero. Input ports are protected to +6V under any of these circumstances (Figure 10).

Driving LED Loads

When driving LEDs from one of the four output ports O0, O1, O6, or O7, a resistor must be connected in series with the LED to limit the LED current to no more than 20mA. Connect the LED cathode to the MAX7322 port, and the LED anode to V+ through the series current-limiting resistor, R_{LED}. Set the port output low to light the LED. Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL}) / I_{LED}$$

where:

R_{LED} is the resistance of the resistor in series with the LED (Ω).

V_{SUPPLY} is the supply voltage used to drive the LED (V).

V_{LED} is the forward voltage of the LED (V).

V_{OL} is the output low voltage of the MAX7322 when sinking I_{LED} (V).

I_{LED} is the desired operating current of the LED (A).

For example, to operate a 2.2V red LED at 10mA from a +5V supply:

$$R_{LED} = (5 - 2.2 - 0.07) / 0.010 = 270\Omega$$

Driving Load Currents Higher than 20mA

The MAX7322 can be used to drive loads, such as relays, that draw more than 20mA by paralleling outputs. Use at least one output per 20mA of load current; for example, a 5V 330mW relay draws 66mA, and therefore, requires all four paralleled outputs. Any combination of outputs can be used as part of a load-sharing design, because any combination of ports can be set or cleared at the same time by writing to the MAX7322. Do not exceed a total sink current of 100mA for the device.

The MAX7322 must be protected from the negative voltage transient generated when switching off inductive loads (such as relays), by connecting a reverse-biased diode across the inductive load. Choose the peak current for the diode to be greater than the inductive load's operating current.

Power-Supply Considerations

The MAX7322 operates with a supply voltage of +1.71V to +5.5V over the -40°C to +125°C temperature range. Bypass the supply to GND with a ceramic capacitor of at least 0.047µF as close to the device as possible. For the TQFN version, additionally connect the exposed pad to GND.

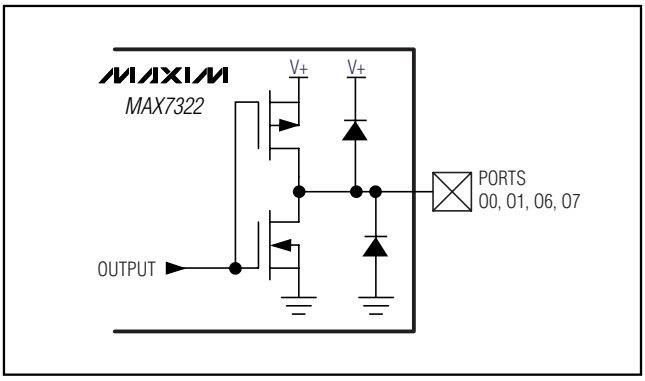


Figure 9. MAX7322 Push-Pull Output Port Structure

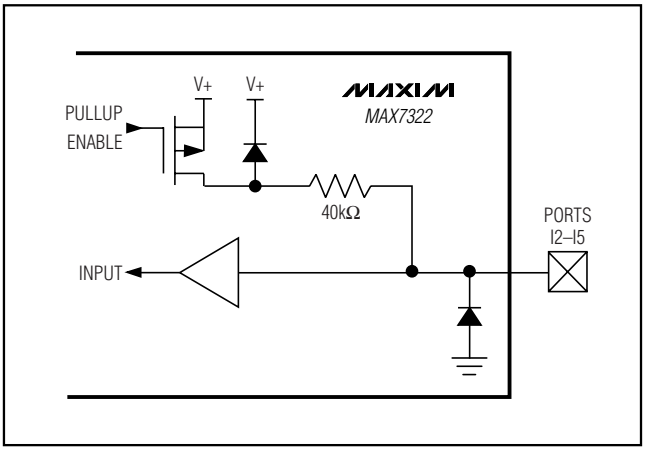
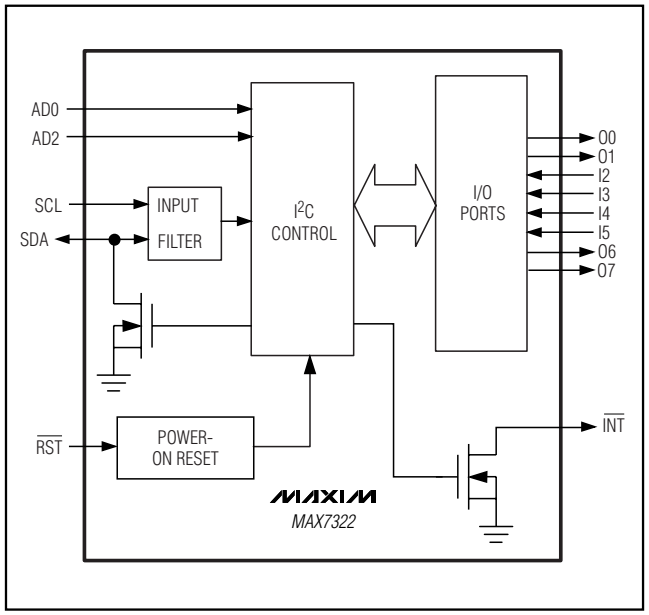


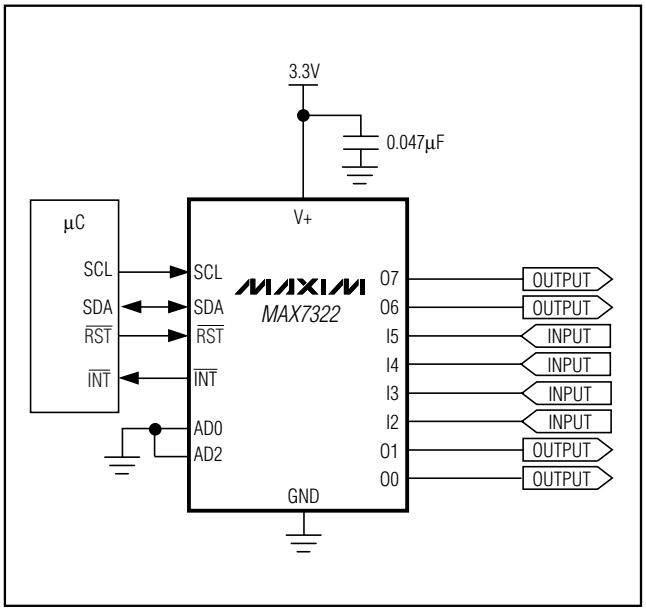
Figure 10. MAX7322 Input Port Structure

I²C Port Expander with 4 Push-Pull Outputs and 4 Inputs

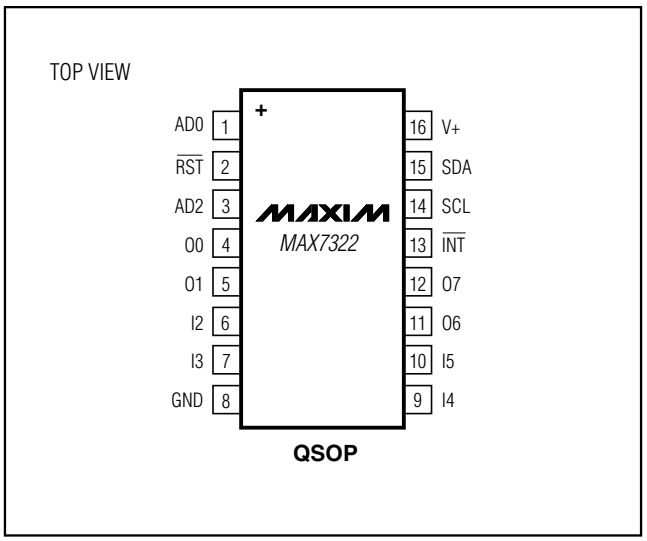
Functional Diagram



Typical Application Circuit



Pin Configurations (continued)



Chip Information

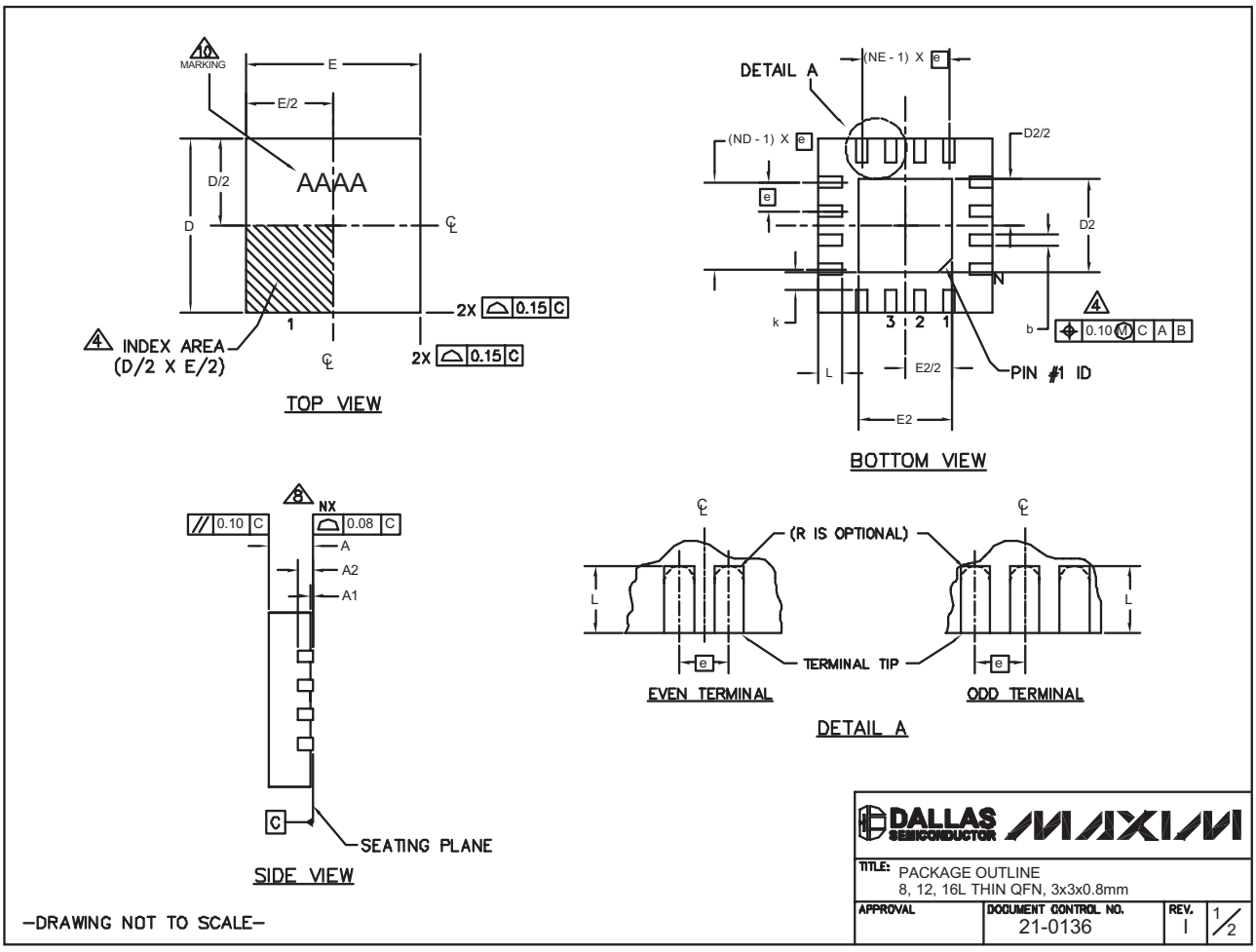
PROCESS: BiCMOS

I2C Port Expander with 4 Push-Pull Outputs and 4 Inputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm

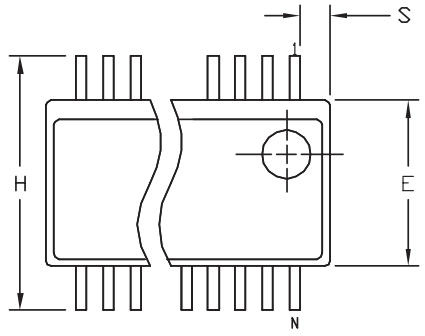
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	I	2/2

I²C Port Expander with 4 Push-Pull Outputs and 4 Inputs

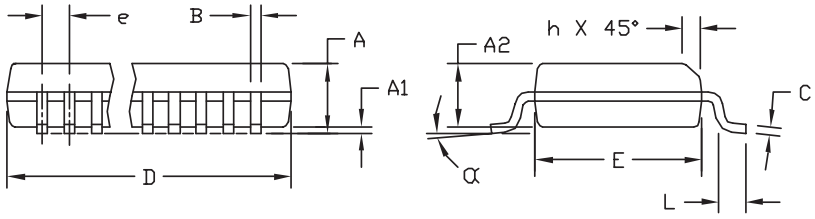
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	F	1/1

Revision History

Pages changed at Rev 1: 1–18