6A, 700kHz Synchronous DC/DC Step-Down Converter

General Description

The RT8085A is a high efficiency switching converter for applications operating input voltage from 2.95V to 5.5V and requiring up to 6A maximum load. This single-chip converter provides extremely compact, fast and accurate power delivery solutions for low output voltage applications. The RT8085A provides the reference input REFIN to allow a dynamic output voltage change. The RT8085A automatically switches from Continuous Conduction Mode (CCM) to Discontinuous Conduction Mode (DCM) for light load efficiency.

Ordering Information

RT8085A □□

Package Type
QW : WDFN-12L 3x3 (W-Type)
(Exposed Pad-Option 1)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

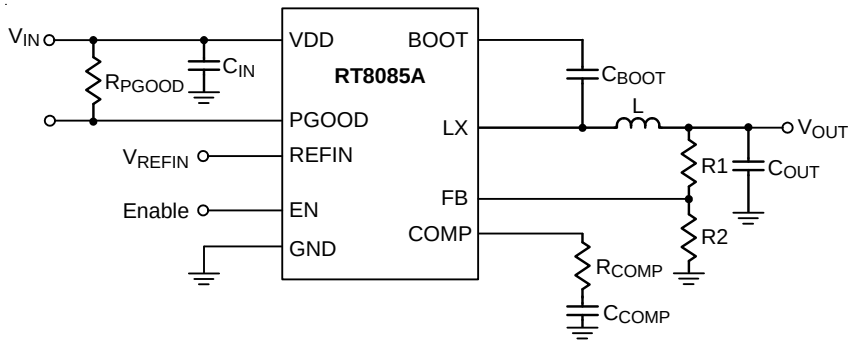
Features

- **External Reference Input REFIN**
- **Low On-Resistance**
  - **38mΩ of High-Side MOSFET**
  - **20mΩ of Low-Side MOSFET**
- **DCM Operation for Light Load Efficiency**
- **Support MLCC Capacitors**
- **700kHz Switching Frequency**
- **Power Good Indictor**
- **Enable Control**
- **Cycle-by-Cycle Current Limit**
- **Short-Circuit Protection**
- **Latch Off UVP**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Point of Load Voltage Regulators
- Notebook
- Ultrabook
- Tablet PCs
- Portable Devices

Simplified Application Circuit



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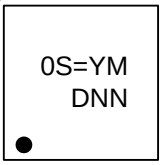
Marking Information

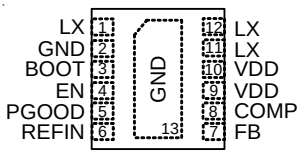


0S= : Product Code

YMDNN : Date Code

Pin Configurations

(TOP VIEW)

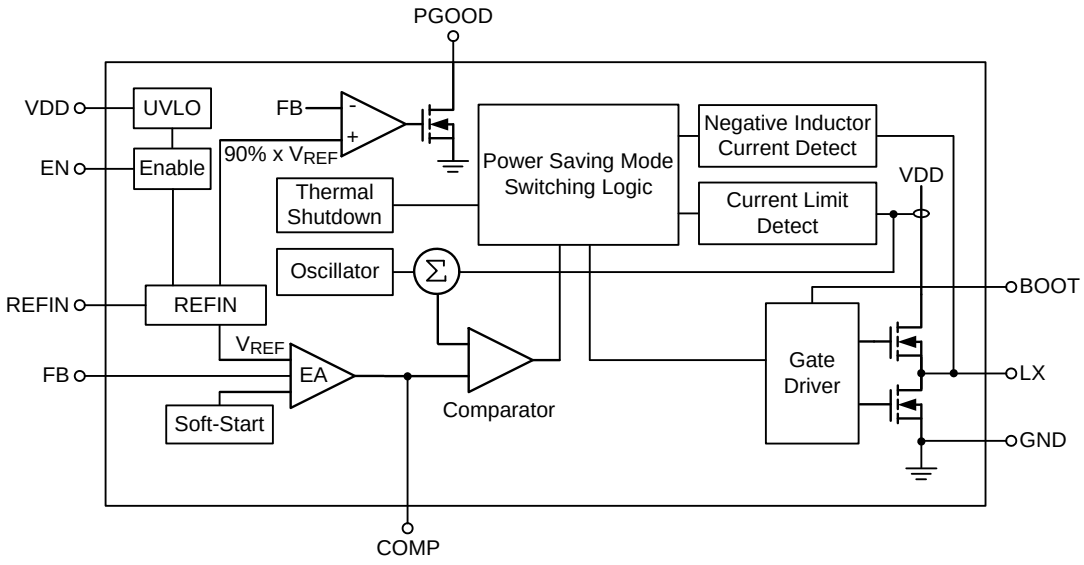


WDFN-12L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 11, 12	LX	Switch Node. Connect the switch node to the output inductor.
2, 13 (Exposed Pad)	GND	Power Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	BOOT	Bootstrap Supply for High-Side Gate Driver. This pin powers the high-side MOSFET driver. Connect a 0.1μF capacitor between the BOOT and LX pins.
4	EN	Enable Control Input. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to VDD enables the device. This pin must not be left floating and must be terminated.
5	PGOOD	Power Good Indicator Output (Open-Drain). A 100kΩ pull-high resistor is required.
6	REFIN	External Reference Input.
7	FB	Feedback Voltage Input. This pin receives the feedback voltage from a resistive divider connected across the output.
8	COMP	Compensation Node. Connect external compensation elements to this pin to stabilize the control loop.
9, 10	VDD	Power Input.

Function Block Diagram



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Operation

The RT8085A is a current-mode synchronous step-down DC/DC converter with two integrated power MOSFETs. It can deliver up to 6A output current from a 2.95V to 5.5V input supply, and provide an reference input voltage ranging from 0.6V to 2V. The RT8085A's current-mode architecture allows the transient response to be optimized over a wide input voltage and load range. Cycle-by-cycle current limit provides protection against shorted outputs, and soft-start eliminates input current surge during start-up.

Error Amplifier

The error amplifier adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal reference voltage 0.6V at stand-alone mode or reference input voltage at tracking mode. When the load current increases, it causes a drop in the feedback voltage relative to the reference. The COMP voltage then rises to allow higher inductor current to match the load current.

Enable

The converter is turned on when the EN pin is higher than 0.7V. When the EN pin is lower than 0.4V, the converter will enter shutdown mode and reduce the supply current to 0.1μA.

Soft-Start (SS)

An internal current source charges an internal capacitor to build a soft-start ramp voltage. The FB voltage will track the internal ramp voltage during soft-start interval. For different reference input voltages, the soft-start time is also different. The typical soft-start time is 2ms when reference input voltage is 1V.

Thermal Shutdown

The thermal shutdown function shuts down the switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will automatically resume switching.

PGOOD Comparator

When the feedback voltage (V_{FB}) rises above 90%, the PGOOD open-drain output will be high impedance. The PGOOD open-drain output will be internally pulled low when the feedback voltage (V_{FB}) falls below 85% of reference voltage at stand-alone mode and 65% of reference voltage at tracking mode.

UV Comparator

If the feedback voltage (V_{FB}) is lower than 65% reference voltage at stand-alone mode or 35% reference input voltage at tracking mode, the UV comparator will go high to turn off the high-side MOSFET and the low-side MOSFET. The output under-voltage protection is designed to operate in latch mode. When the UV condition is removed, the converter needs to re-soft-start.

VOUT Over-Voltage Comparator

If the feedback voltage (V_{FB}) is over 125% reference voltage at stand-alone mode or 165% reference input voltage at tracking mode, the VOUT over voltage comparator will go high to turn off the high-side MOSFET and turn on the low-side MOSFET until entering UV-latch mode.

REFIN Operation

When IC is power-on, there is a blanking time about 500μs to decide the operation mode before starting switching. If the reference input voltage is lower than 0.6V, IC enters stand-alone mode and the reference voltage is internal reference 0.6V. If the reference input voltage is between 0.6V and 2V, IC enters tracking mode and the reference voltage is followed by the reference input. The operating mode is fixed after the blanking time is over. It needs to re-soft-start for adjusting REFIN mode.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD ---------- –0.3V to 6V
- LX to GND ---------- –0.3V to 6V
- BOOT to GND ---------- –0.3V to 12V
- Other Pins ---------- –0.3V to (V_{DD} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-12L 3x3 ---------- 3.28W
- Package Thermal Resistance (Note 2)
  WDFN-12L 3x3, θ_{JA} ---------- 30.5°C/W
  WDFN-12L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 2.95V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage		V_{REF}	V_{REFIN} = 0V	0.594	0.6	0.606	V
			V_{REFIN} = 0.6V	0.594	0.6	0.606	
Reference Input Voltage Range		V_{REFIN}	Stand-alone Mode (V_{REF} = 0.6V)	--	--	0.4	V
			Tracking Mode	0.6	--	2	
Reference Voltage Step Response Slew Rate		S_{TR}	Rising Slew Rate, V_{REF} from 5% to 95%	--	30	--	mV/μs
		S_{TF}	Falling Slew Rate, V_{REF} from 95% to 5%	--	30	--	
Quiescent Current		I_Q	No Switching	--	350	--	μA
Shutdown Current		I_{SHDN}	V_{EN} = 0V, V_{LX} = 0V	--	0.1	1	μA
Under-Voltage Lockout Threshold		V_{UVLO}	Rising	2.55	2.8	2.95	V
			Falling	2.35	2.625	2.8	
EN Input Voltage	Logic-High	V_{IH}	V_{DD} = 2.95V to 5.5V	0.7	--	V_{DD}	V
	Logic-Low	V_{IL}	V_{DD} = 2.95V to 5.5V	--	--	0.4	
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		T_{SD_HYS}		--	20	--	°C

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Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Switch On-Resistance	$R_{DS(ON)\_H}$	High-Side, I_{LX} = 0.2A, V_{DD} = 5V		--	38	--	mΩ
	$R_{DS(ON)\_L}$	Low-Side, I_{LX} = 0.2A, V_{DD} = 5V		--	20	--	
Output Line Regulation		V_{DD} = 2.95V to 5.5V		--	0.5	--	%
Output Load Regulation		0A < I_{LOAD} < 6A		--	0.5	--	%
Power Good Threshold	V_{PGOOD}	V_{FB} Rising		85	90	--	%
		V_{FB} Falling	Stand-alone Mode	--	85	92	
			Tracking Mode	--	65	72	
Oscillator Frequency	f_{OSC}	V_{DD} = 5V		--	700	--	kHz
Current Limit	I_{OC}	High-Side MOSFET Peak Current		7.8	9	--	A
Soft-Start Time	T_{SS}	V_{REFIN} = 1V		--	2	--	ms
Over-Voltage Protection	V_{OVP}	Stand-alone Mode		--	125	--	%
		Tracking Mode		--	165	--	
Under-Voltage Protection	V_{UVP}	Stand-alone Mode		--	65	--	%
		Tracking Mode		--	35	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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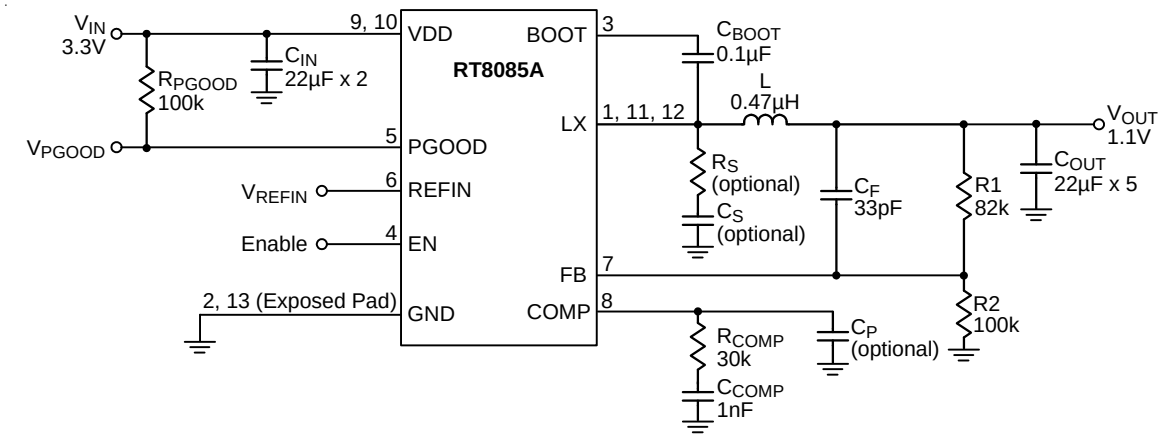
Typical Application Circuit



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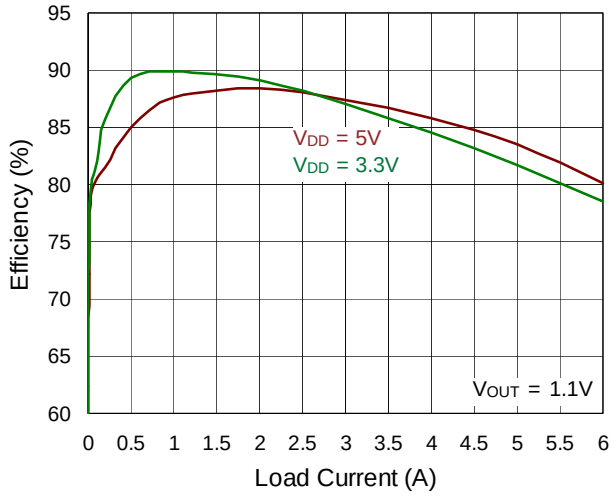
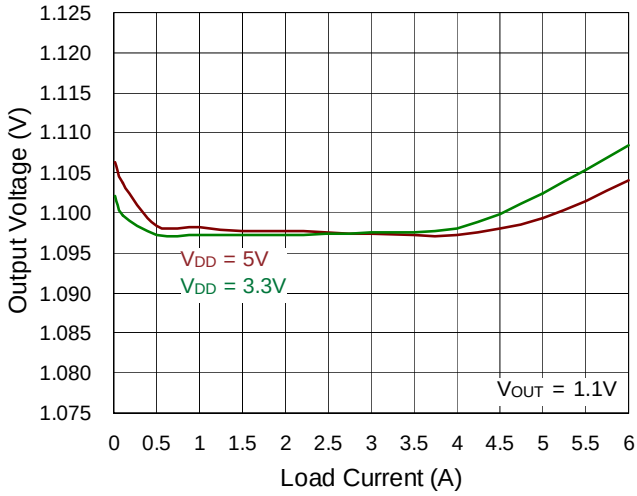
Typical Operating Characteristics

V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified.

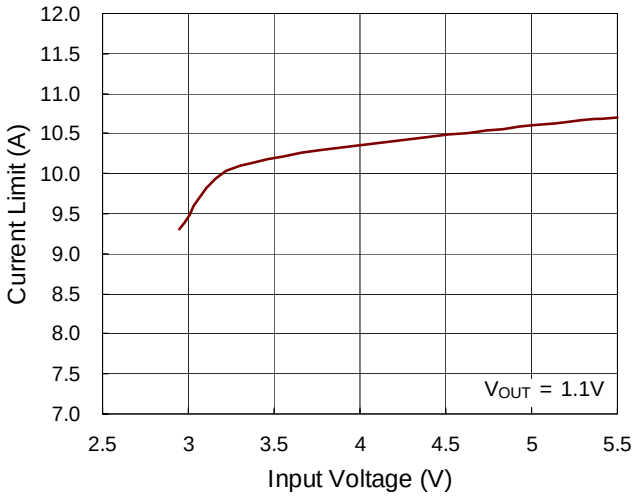
Efficiency vs. Load Current



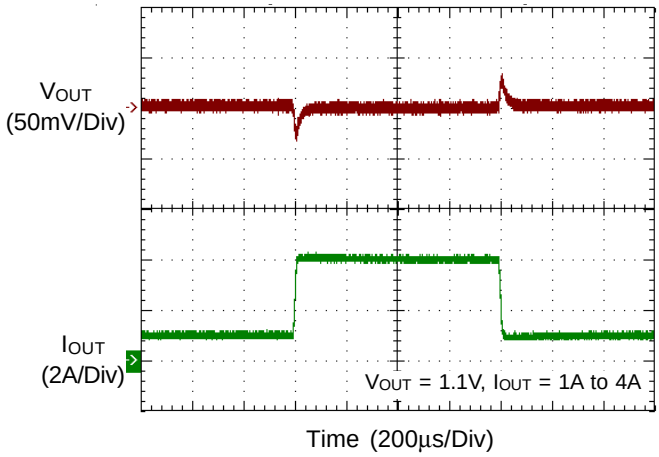
Output Voltage vs. Load Current



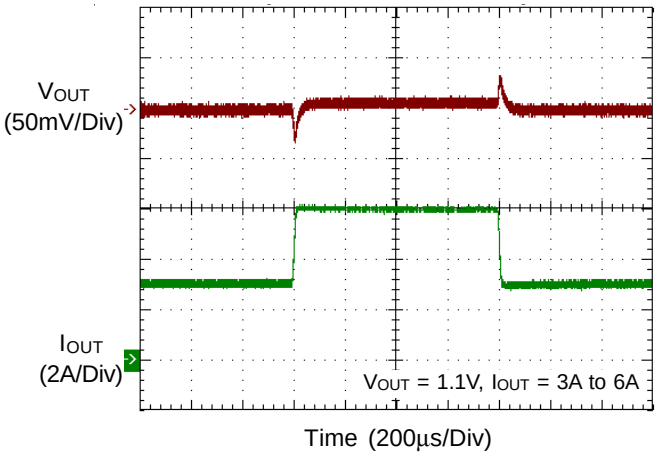
Current Limit vs. Input Voltage



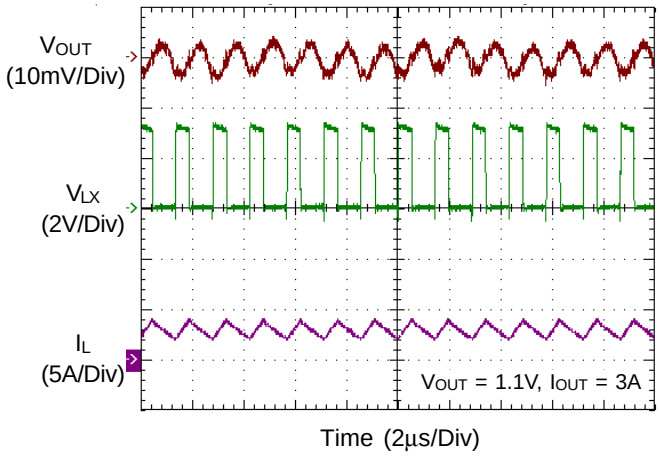
Load Transient Response



Load Transient Response



Output Voltage Ripple



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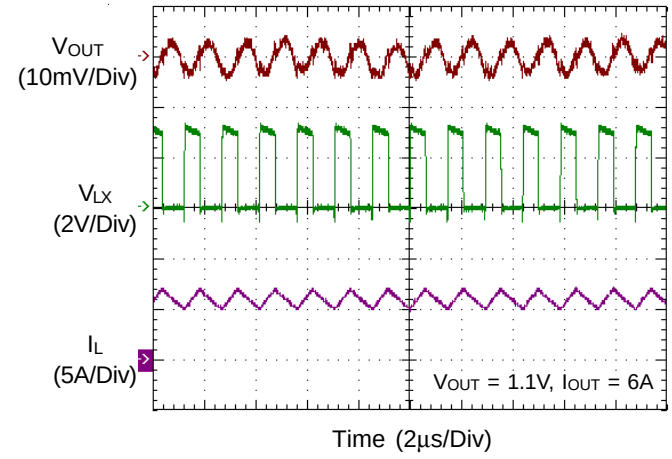
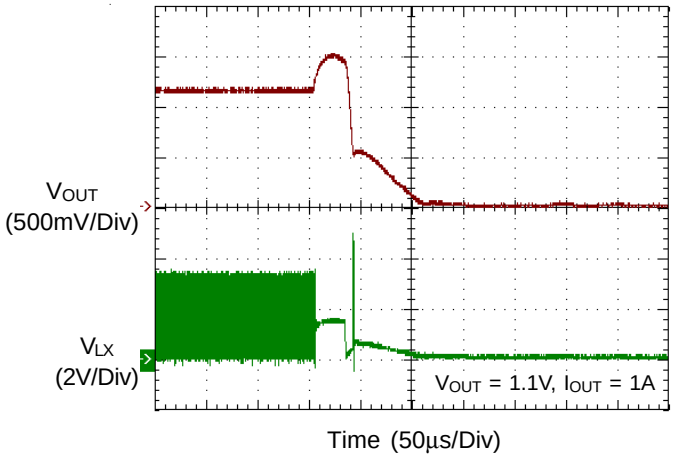
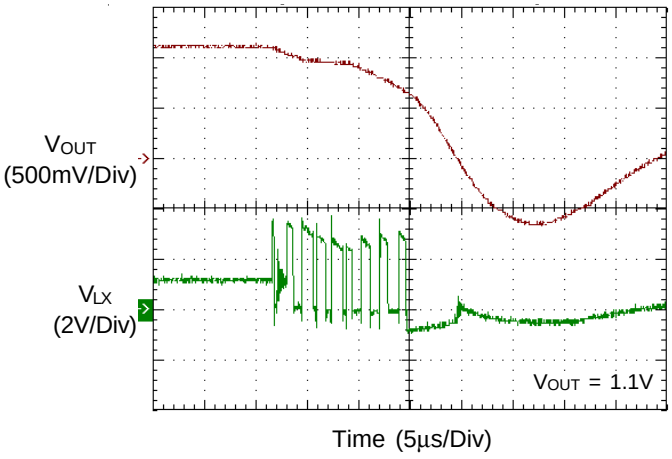
Output Voltage Ripple



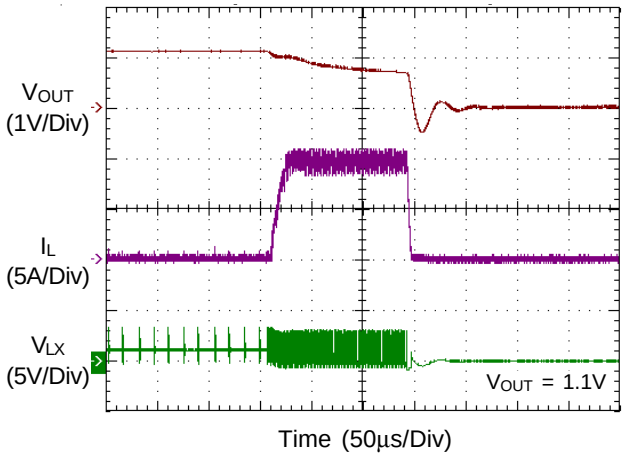
Over-Voltage Protection



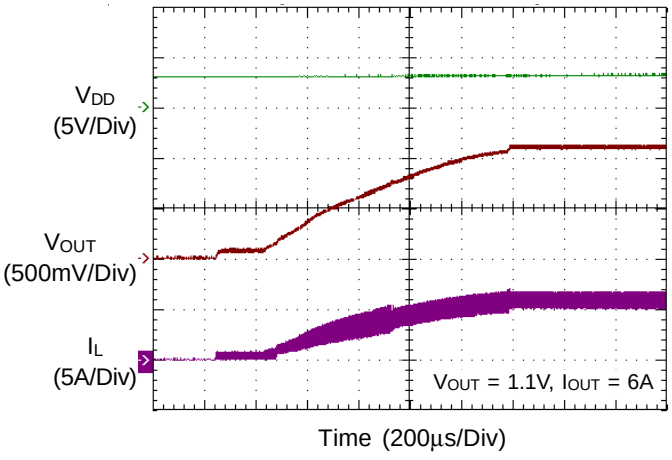
Under-Voltage Protection



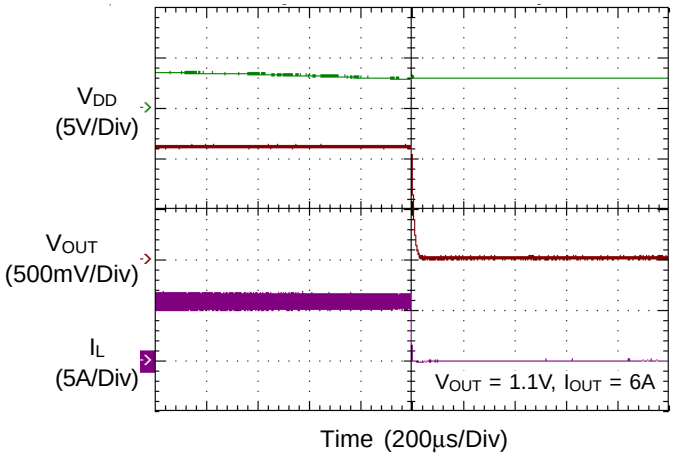
Over-Current Protection



Power On from VDD



Power Off from VDD



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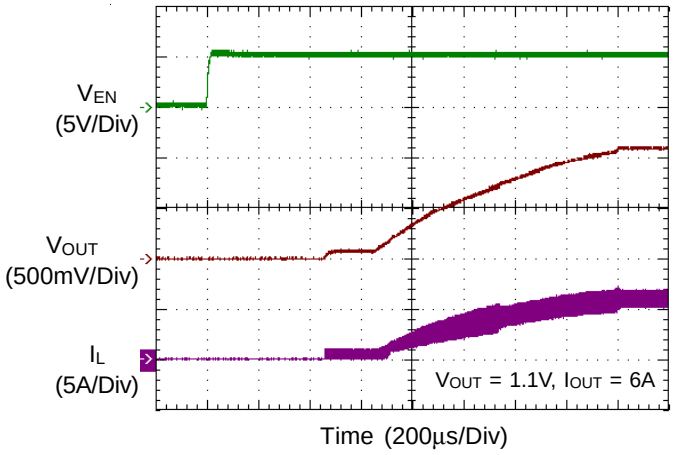
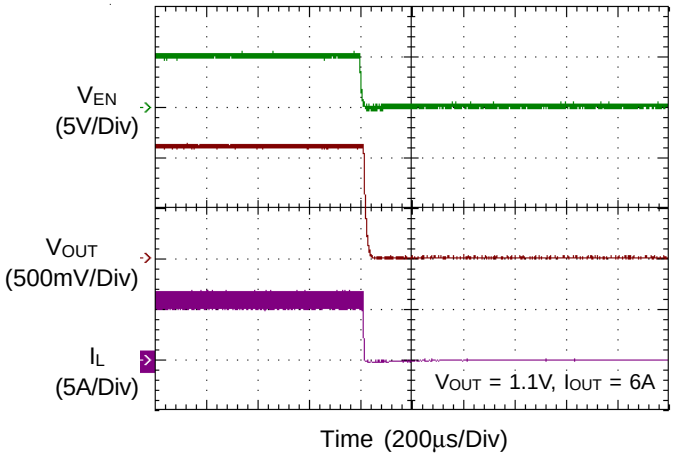
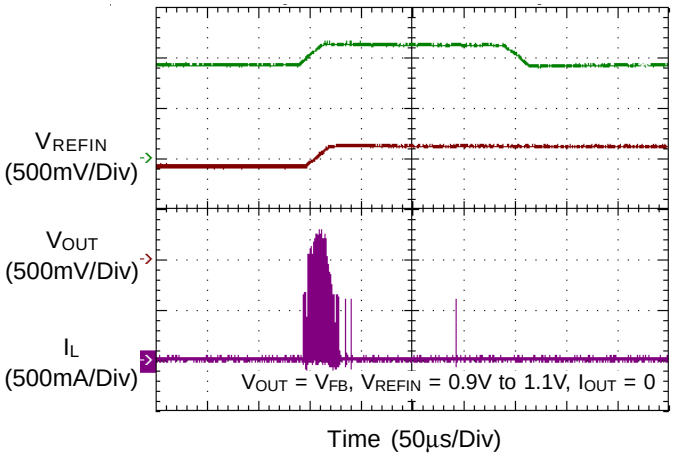
Power On from EN



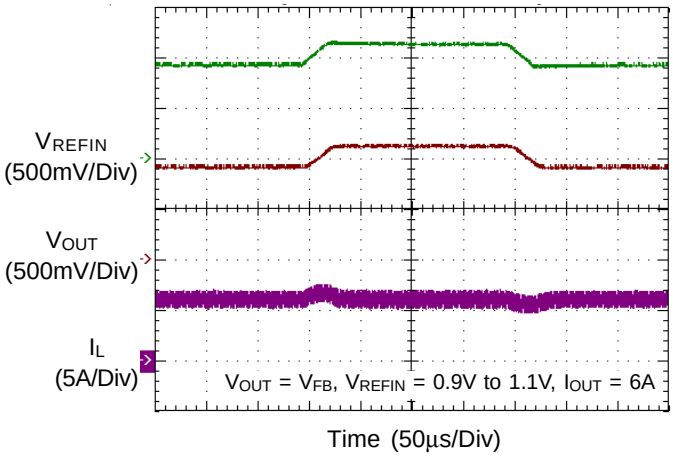
Power Off from EN



REFIN Transient Response



REFIN Transient Response



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Application Information

The RT8085A is a single-phase Buck converter. It provides single feedback loop, current-mode control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated at a fixed output voltage. An external reference ranging from 0.6V to 2V also supports the output voltage to be dynamically changed. Protection features include over-current protection, under-voltage protection, over-voltage protection and over-temperature protection.

Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where V_{REF} is the reference voltage.

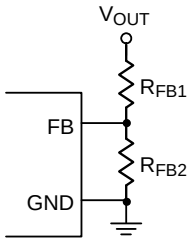

Figure 1. Setting V_{OUT} with a Voltage Divider

Notice that the maximum duty cycle should be less than 93%.

Reference Mode Selection

The RT8085A has two reference modes : stand-alone mode and tracking mode. When the REFIN pin is tied to lower than 0.6V, the chip will operate in the stand-alone mode, and the reference voltage will be fixed at 0.6V. If the REFIN is connected to a voltage ranging from 0.6V to 2V, the chip will operate in the tracking mode, and the reference voltage can be dynamically changed through the REFIN pin with a maximum 30mV/μs changing slew rate. During the REFIN falling stage, the RT8085A will not switch to discharge the output voltage. Therefore, the maximum REFIN falling step should be less than 165% of target level to avoid triggering OVP. Notice that the mode selection should be set before the chip is powered on.

Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT8085A remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the V_{EN} trip point, the RT8085A begins a new initialization and soft-start cycle.

Internal Soft-Start

The RT8085A provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled and blanking time for reference mode is over. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the output surge current. The internal reference takes over the loop control once the internal ramping-up voltage becomes higher than reference voltage.

UVLO Protection

The RT8085A has input Under-Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.8V typ.), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

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Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough and not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 20µF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{IN\_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select a proper capacitor for RMS current rating. One good design uses more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times V_{OUT}}{C_{IN} \times f_{SW}}$$

For example, if V_{IN} = 5V, V_{OUT} = 1.05V, $I_{OUT(MAX)}$ = 6A, C_{IN} = 22µF, f_{SW} = 700kHz, the input voltage ripple will be 82mV.

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the Buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (V_{P-P}) can be calculated by the following equation :

$$V_{P\_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage undershoot (V_{SAG}) can be calculated by the following equation :

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Unlike the electrolytic capacitor, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, use a mixed combination of electrolytic capacitor and ceramic capacitor to obtain better transient performance.

Power Good Output (PGOOD)

PGOOD is an open-drain type output and requires a pull-up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. It is released when the output voltage rises above 90% of nominal regulation point. The PGOOD signal goes low if the output is turned off or is 15% and 35% below its nominal regulation point in Stand-alone mode and Tracking mode, respectively.

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Under-Voltage Protection (UVP)

The output voltage can be continuously monitored for under-voltage. When under-voltage protection is enabled, both UGATE and LGATE gate drivers will be forced low if the output is less than 65% and 35% of its set voltage threshold in stand-alone mode and tracking mode, respectively. The UVP will be ignored in soft-start period. Toggle EN threshold or cycle V_{IN} to reset the UVP fault latch and restart the controller.

Over-Voltage Protection (OVP)

The over-voltage protection monitors the output voltage via the FB pin. If the output voltage exceeds 25% and 65% of its set voltage threshold in stand-alone mode and tracking mode, respectively, over-voltage protection will be triggered. The RT8085A is latched once OVP is triggered and can only be released by toggling EN threshold or cycling V_{IN}.

Over-Current Protection (OCP)

The RT8085A provides over current protection by detecting high side MOSFET peak inductor current. If the sensed peak inductor current is over the current limit threshold (9A typ.), the OCP will be triggered. When OCP is tripped, the RT8085A will keep the over-current threshold level until the over-current condition is removed.

Thermal Shutdown (OTP)

The device implements an internal thermal shutdown function when the junction temperature exceeds 150°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal shutdown threshold. Once the die temperature decreases below the hysteresis of 20°C, the device reinstates the power-up sequence.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-12L 3x3 packages, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (30.5°C/W) = 3.28W for WDFN-12L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

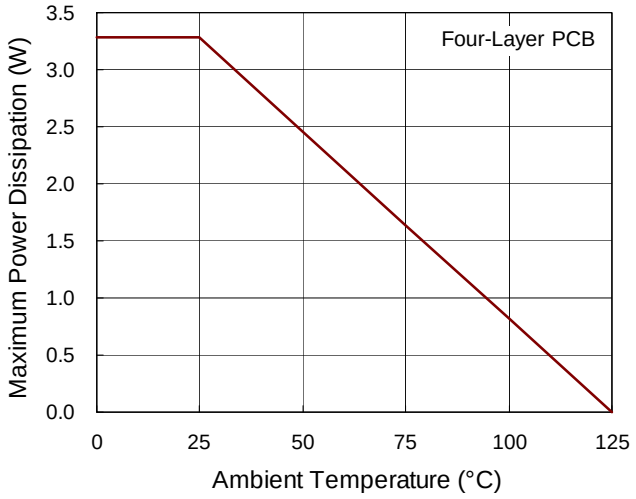

Figure 2. Derating Curve of Maximum Power Dissipation

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Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout. Certain points must be considered before starting a layout using the RT8085A.

- Make the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VDD and GND).
- LX node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the LX node to prevent stray capacitive noise pick-up.
- Ensure all feedback network connections are short and direct. Place the feedback network as close to the chip as possible.
- The GND pin and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.
- An example of PCB layout guide is shown in Figure 3. for reference.

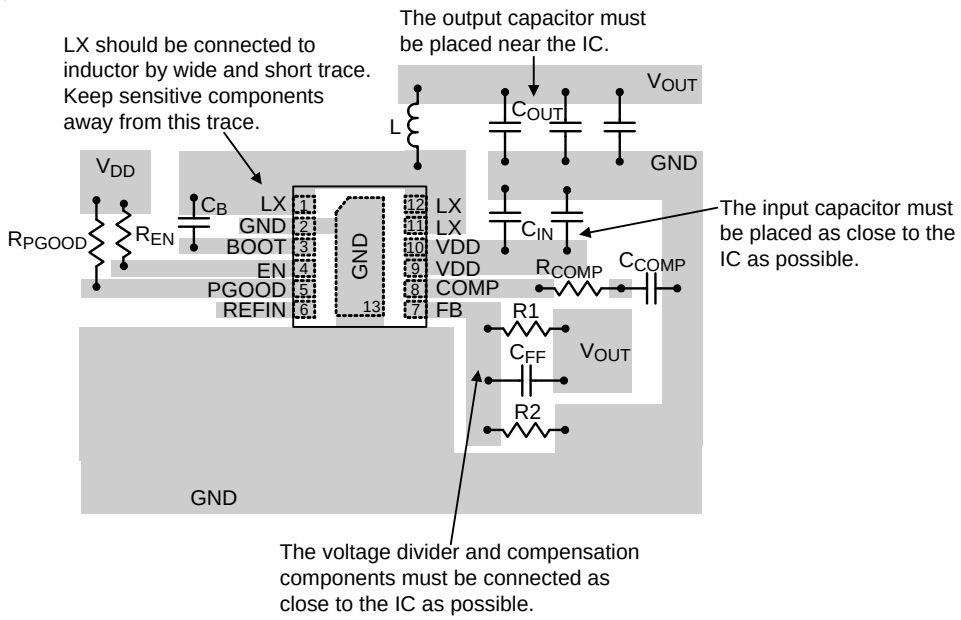

Figure 3. PCB Layout Guide

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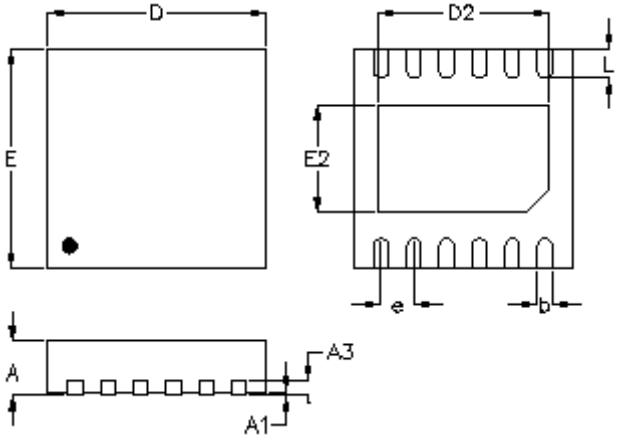
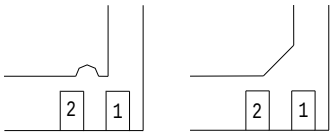
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		2.950	3.050	0.116	0.120
D2	Option1	2.300	2.650	0.091	0.104
	Option2	1.970	2.070	0.078	0.081
E		2.950	3.050	0.116	0.120
E2	Option1	1.400	1.750	0.055	0.069
	Option2	1.160	1.260	0.046	0.050
e		0.450		0.018	
L		0.350	0.450	0.014	0.018

W-Type 12L DFN 3x3 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

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