PIC16F87/88

PIC16F87/88 Rev. B1 Silicon Errata

The PIC16F87/88 Rev. B1 parts you have received conform functionally to the Device Data Sheet (DS30487**C**), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC16F87/88 silicon.

The following silicon errata apply only to PIC16F87/88 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F87	00 0111 001	0 0101
PIC16F88	00 0111 011	0 0101

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

1. Module: Internal RC Oscillator

A high Sleep current will exist when the following condition is met and procedures are followed:

CONDITION: FOSC<2:0> (Configuration Word 1 Register) bits are configured for any oscillator selection other than the internal RC oscillator.

PROCEDURE:

1. Clock switch occurs anywhere in the application code where the internal RC oscillator is selected via the SCS bits ('10').
2. Sleep mode is entered while the SCS bits are configured for the internal RC oscillator ('10').

Work around

Before Sleep mode is entered, configure or clear the SCS bits ('00') to switch back to the primary clock source that is defined by FOSC<2:0> (Configuration Word 1 Register).

Date Codes that pertain to this issue:

All date codes associated with silicon revision B1. This issue is not found in devices with silicon revision C2 (Revision ID 01000) or later.

2. Module: Internal RC Oscillator IOFS bit

The device data sheet states when an INTOSC frequency is selected (125, 250, 500 kHz; 1, 2, 4, 8 MHz), the frequency will be stable when the IOFS bit becomes set (IOFS = 1) at 4 ms. The following applies for applications relying on time dependent code.

Under the following conditions, any of the INTOSC frequencies may not be stable when IOFS becomes set (IOFS = 1). Devices may vary from one to the next and may take as long as 60 ms to become stable.

1. Wake from Sleep, internal RC oscillator is selected via the SCS bits or Configuration Word 1 and the IRCF bits are configured for an INTOSC frequency.
2. POR is executed, internal RC oscillator is selected via the SCS bits or Configuration Word 1 and the IRCF bits are configured for an INTOSC frequency.
3. The INTRC (31.25 kHz) is clocking the device and a switch to an INTOSC frequency is executed via modification of the IRCF bits.
4. An alternative oscillator selection is clocking the device (i.e., HS mode) and a clock switch to the internal RC oscillator is executed via the SCS bits with the IRCF bits configured for an INTOSC frequency.

Work around

Implement the following software delay shown in Example 1 after an INTOSC frequency has been enabled and before any frequency dependent application code is executed. This routine will delay application execution approximately 2K-150K TCY (instruction cycles are dependent upon the INTOSC frequency) to ensure a stable INTOSC frequency.

Date Codes that pertain to this issue:

All date codes associated with silicon revision B1. This issue is not found in devices with silicon revision C2 (Revision ID 01000) or later.

EXAMPLE 1: DELAY ROUTINE

```
DlyVarH    equ    <define address based on application requirements>
DlyVarL    equ    <define address based on application requirements>

;Load the delay variable DlyVarH with the following value for the selected frequency:
    ;125kHz   0x0300
    ;250kHz   0x0600
    ;500kHz   0x0C00
    ;1MHz     0x1900
    ;2MHz     0x3100
    ;4MHz     0x6200

delay                       ;insure the correct data memory bank is selected
                            ; for access of data variables
    CLRF      DlyVarL       ;initialize low delay variable
    MOVLW     0x62          ;initialize high delay variable
    MOVWF     DlyVarH

dly_loop
    DECFSZ    DlyVarL,f     ;decrement low variable
    GOTO      dly_loop
    DECFSZ    DlyVarH,f     ;decrement high variable
    GOTO      dly_loop
RETURN                      ;delay done
```

3. Module: Internal RC Oscillator

When any one of the seven INTOSC frequencies is enabled by the following conditions, it is possible for the oscillator to overshoot the selected frequency:

1. A clock switch from INTRC (31 kHz) to an INTOSC (125 kHz-8 MHz) frequency via the IRCF bits (OSCCON register).
2. Exit from Sleep mode with the IRCF bits already configured for an INTOSC frequency.
3. Executing a clock source switch via the SCS bits (OSCCON register) to the internal RC oscillator with the IRCF bits already configured for an INTOSC frequency.

If the selected frequency is 8 MHz, then the voltage versus frequency specification of the device may be violated.

Work around

When it is required for the application to run at 8 MHz, it is recommended that the application does not start executing code at 8 MHz until the 60 ms firmware delay (see issue 2) has completed. During the 60 ms settling period, the application can execute code up to 4 MHz. Upon completion of the 60 ms firmware delay, the 8 MHz can be selected via the IRCF bits.

Date Codes that pertain to this issue:

All date codes associated with silicon revision B1. This issue is not found in devices with silicon revision C2 (Revision ID 0 1000) or later.

4. Module: PORTB Pull-ups

When $\overline{\text{RBPU}}$ = 0 (OPTION_REG register), the PORTB weak pull-ups will not be disabled by the input functions of the SSP and/or CCP (Capture mode) module as indicated by the RB<5:1> I/O block diagrams in **Section 5.0 "I/O Ports"**.

Work around

1. If the SSP and/or CCP (Capture mode) module is enabled, do not enable the PORTB weak pull-ups and use external pull-up resistors.

OR

2. If the SSP and/or CCP (Capture mode) module and PORTB pull-ups are enabled, then evaluate the functionality of the SSP (I^2C™/SPI) or CCP (Capture mode) module to ensure proper operation within your application.

Date Codes that pertain to this issue:

All date codes associated with silicon revision B1. This issue is not found in devices with silicon revision C2 (Revision ID 0 1000) or later.

5. Module: PORTB

A delay of 1 TOSC will occur if an instruction that modifies the contents of PORTB simultaneously occurs when any of the following modules (if enabled) execute an operation that effects the signals on their respective PORTB I/O pins.

CCP Module:
PWM Mode (CCP1CON<3:0> = 11xx)

When CCP1CON<5:4> bits = 10, the PWM output signal will be delayed by 1 TOSC when an instruction to modify the contents of PORTB is executed.

SSP Module:
SPI Slave Modes (SSPCON<3:0> = 0100 and 0101)

Clock signal is derived from an external source. Transmission of data (SDO pin) will be delayed by 1 TOSC when an instruction to modify the contents of PORTB is executed. Reception of data is not affected.

AUSART Module:
Synchronous Slave Mode (TXSTA<7> = 0)

Clock signal is derived from an external source. Transmission of data (TX pin) will be delayed by 1 TOSC when an instruction to modify the contents of PORTB is executed. Reception of data is not affected.

Work around

None

Date Codes that pertain to this issue:

All date codes associated with silicon revision B1. This issue is not found in devices with silicon revision C2 (Revision ID 0 1000) or later.

6. Module: PORTB, RB6 Pin

During normal operating conditions, extra current will be consumed on the PIC16F87/88 device's power source (V_{DD}) when the PORTB, RB6 pin is configured as an analog input (AN5) and is connected to an analog source. A/D operation on RB6 or any of the other analog I/O pins will not be affected by this extra current. The extra current is due to the T1CKI Schmitt Trigger not being disabled when RB6 is configured as an analog pin. The amount of additional current observed will be dependent on the analog voltage present on the AN5 pin. The following table illustrates this additional current across operating temperatures:

	Max	Units	Conditions		
All Devices	1.4	mA	-40°C	V_{DD} = 5.5V	AN5 = 0.6-0.7 V_{DD}
	1.3	mA	+25°C		
	1.1	mA	+85°C		
Extended Devices	0.9	mA	+125°C		

Work around

None

Date Codes that pertain to this issue:

All date codes associated with silicon revision B1. This issue is not found in devices with silicon revision C2 (Revision ID 0 1000) or later.

7. Module: PORTB Interrupts

When the PORTB interrupt-on-change feature and a PORTB peripheral are enabled simultaneously, the PORTB peripheral input signal's rising and falling edges will trigger an interrupt-on-change event. This is due to the interrupt-on-change feature not being disabled on the respective pin for that peripheral when it is enabled.

The affected pins and peripheral signals on PORTB are RB4: SCK and SCL, RB5: $\overline{SS}$ and RB6: T1CKI. The functionality of T1OSI (RB7), T1OSO (RB6) and TX/CK (RB5) is not affected by this issue.

Work around

None

Date Codes that pertain to this issue:

All date codes associated with silicon revision B1. This issue is not found in devices with silicon revision C2 (Revision ID 0 1000) or later.

8. Module: Oscillator Configurations (OSCTUNE Register)

The Device Data Sheet has been revised to reflect changes in the operation of the OSCTUNE register, beginning with silicon Revision C0. The following text and table describe that register's implementation for silicon Revision B1.

The OSCTUNE register adjusts the frequencies of the INTOSC and INTRC clock sources.

OSCTUNE bit 0 is implemented. When the register is modified, the INTOSC and INTRC frequencies begin shifting to the new frequency. The INTRC clock reaches the new frequency within eight clock cycles (approximately 8 * 32 μs or 256 μs).

Work around

N/A

Date Codes that pertain to this issue:

All date codes associated with silicon revision B1. This issue is not found in devices with silicon revision C2 (Revision ID 0 1000) or later.

REGISTER 4-1: OSCTUNE: OSCILLATOR TUNING REGISTER (ADDRESS 90h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** Frequency Tuning bits

011111 = Maximum frequency
011110 =
•
•
•
000001 =
000000 = Center frequency. Oscillator module is running at the calibrated frequency.
111111 =
•
•
•
100000 = Minimum frequency

REVISION HISTORY

Rev A Document (9/2003)
First revision of this document. Data Sheet Clarification issue 1 (Voltage Reference Specifications).

Rev B Document (2/2004)
Added Data Sheet Clarification issue 2 (Timer1 Oscillator and In-Circuit Serial Programming).

Rev C Document (4/2004)
Added silicon issue 1 (Internal RC Oscillator).

Rev D Document (6/2004)
Updated silicon issue 1 (Internal RC Oscillator) and added Data Sheet Clarification issue 3 (DC Characteristics).

Rev E Document (9/2004)
Added silicon issue 2 (Internal RC Oscillator IOFS bit) and 3 (PORTB Pull-ups).

Rev F Document (10/2004)
Amended silicon issue 1 (Internal RC Oscillator) and 2 (Internal RC Oscillator IOFS bit), added new issue 3 (Internal RC Oscillator), renumbered existing issue 3 to issue 4 (PORTB Pull-ups) and added issue 5 (PORTB).

Rev G Document (2/2005)
Removed Data Sheet Clarification issues.

Rev H Document (4/2005)
Added silicon issue 6 (PORTB, RB6 pin).

Rev J Document (6/2005)
Added silicon issue 7 (PORTB Interrupts).

Rev K Document (9/2006)
Annotated all silicon issues to show resolution in subsequent silicon revisions of this device.

Rev L Document (1/2008)
Added silicon issue 8 (Oscillator Configurations, OSCTUNE Register).

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