

# **Application Note**

**Surface Mounted synchronized rectifier type Chopper Regulator IC**

**SI-8205NHG**

November. 2014 Rev.3.0

**SANKEN ELECTRIC CO., LTD.**

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## 1. General Description

The SI-8205NHG is a synchronized rectifier type chopper regulator IC with a built-in power MOS. Due to a current control system, it is applicable to such a super low ESR capacitor as a ceramic capacitor. It is provided with various protection functions such as overcurrent protection, low input prohibition, overheat protection etc. In order to protect the IC against in-rush current at start-up, the soft start function is provided. The soft start time can be set by connecting external capacitors. In addition, the internal oscillator can be operated in 300 kHz to 1MHz by external signals. This device is supplied in a compact and thin HSOP 8-pin package with heat slug on the back side.

### **•1-1 Features**

- Output current 3.0A  
The output current of each output is maximum 3.0A in the HSOP 8-pin surface mounting package.
- High efficiency  
Maximum efficiency 94%
- Output voltage variable  
0.5 - 24V
- Low ESR capacitor for output  
The ceramic capacitor can be used.

#### Operating frequency

Frequency fixed mode (SYNC pin = GND): 250kHz

External synchronization mode: 300kHz - 1MHz

- Built-in functions for overcurrent and thermal shutdown  
A current limiting type protection circuit against overcurrent and overheat is built in. (automatic restoration type)
- Soft start function (capable of ON/OFF output)  
By adding an external capacitor, it is possible to delay the rise speed of the output voltage.  
ON/OFF control of the output is also possible.
- Small package (SI-8205NHG)  
HSOP8 pin package with small heat slug

### **•1-2 Applications**

For on-board local power supplies, power supplies for OA equipment, stabilization of secondary output voltage of regulator and power supply for communication equipment.

### **•1-3 Type**

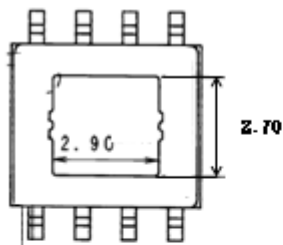
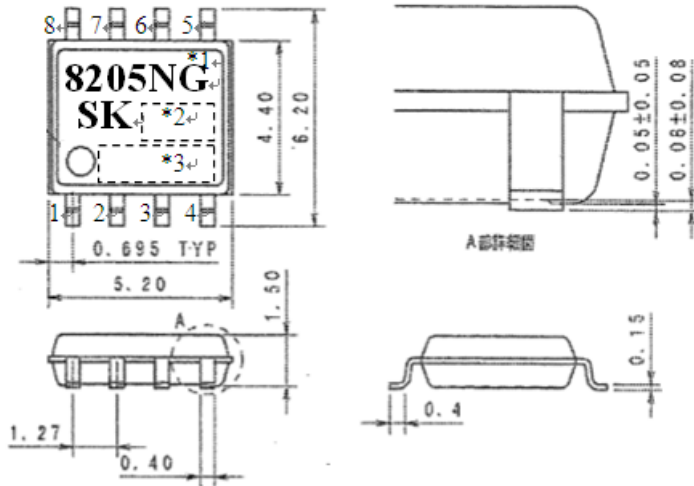
- Type: Semiconductor integrated circuits (monolithic IC)

- Structure: Resin molding type (transfer molding)

## 2. Specification

### ●2-1 Package Information

Unit: mm



\*1 Type number

\*2 Lot number (three digit)

1<sup>st</sup> letter: The last digit of year

2<sup>nd</sup> letter: Month

1 to 9 for Jan. to Sep.

O for Oct.

N for Nov.

D for Dec.

3<sup>rd</sup> and 4<sup>th</sup> letter: week

\*3 Control number (four digit)

#### PIN Assignment

- 1.GND
- 2.EN/SS
- 3.VIN
- 4.SYNC
- 5.COMP
- 6.FB
- 7.BS
- 8.SW

External Terminal Processing: Sn-2.5Ag plating

## ●2-2 Ratings

Table 1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Input Voltage $V_{IN}$	$V_{IN}$	46	V
BS Pin voltage	$V_{BS}$	52	V
BS Pin-SW Pin voltage	$V_{BS-SW}$	6	V
SW Pin voltage	$V_{SW}$	46	V
FB Pin voltage	$V_{FB}$	6	V
EN/SS Pin voltage	$V_{EN/SS}$	6	V
FSET Pin voltage	$V_{FSET}$	6	V
COMP Pin voltage	$V_{COMP}$	6	V
Allowable Power Dissipation *1	$P_d$	1.35	W
Junction Temperature	$T_j$	150	°C
Storage Temperature	$T_{stg}$	-40 to 150	°C
Thermal Resistance (Junction and Case) *2	$\theta_{j-c}$	40	°C /W
Thermal Resistance (Junction and Ambient) *2	$\theta_{j-a}$	74	°C /W

\*1: Since the thermal shutdown is provided, it may be operated at  $T_j > 140^\circ\text{C}$ .

\*2: Glass epoxy board: 30.0mm × 30.0mm (copper foil area: 25.0mm × 25.0mm)

Table 2 Recommended Conditions

Parameter	Symbol	SI-8205NHG	Unit
DC Input Voltage	$V_{IN}$	*3 7v to 43	V
Output Current	$I_o$	0 to 3.0	A
Temperature in Operation	Top	-40 to +85	°C

\*3: The minimum value of input voltage range is 7V or  $V_o + 3V$  whichever higher.

In the case of  $V_{IN} = V_o + 2$  to  $V_o + 3$ ,  $I_{OUT} = 2A$  MAX

Table 3 Electrical Characteristics

(Ta = 25°C, Vo = 5V, R1 = 9kΩ, R2 = 1kΩ)

Parameter		Symbol	Ratings			Unit	Test Condition
			MIN	TYP	MAX		
Setting Reference Voltage		VREF	0.495	0.500	0.505	V	VIN=14V, IO=1.0A
Output Voltage Temperature Coefficient		$\frac{\Delta V_{REF}}{\Delta T}$		±0.05		mV/°C	VIN=14V, IO=1.0A Ta=-40°C to +85°C
Efficiency *4		η		90		%	VIN=14V, Vo=5V, IO=1A
Internal Operation Frequency		fo		250		kHz	VIN=14V, Vo=5V, IO=1A SYNC=GND
Line Regulation *5		VLine		50		mV	VIN=8 to 43V, Vo=5V, IO=1A
Load Regulation *5		VLoad		50		mV	VIN=14V, Vo=5V, IO=0.1 to 3.0A , f=500kHz
Overcurrent Protection Start Current		IS	3.1		6.0	A	VIN=14V, Vo=5V
Circuit Current in Non-operation 1		IIN		12		mA	VIN= 14V, Vcomp=0V
Circuit Current in Non-operation 2		IIN(off)			35	uA	VIN= 14V, VEN/SS= 0V
EN/SS terminal	Flow-out Current at Low Level Voltage	IEN/SS		5		μA	VEN/SS=0V, VIN= 12V
	Open-circuit Voltage	VSSH	3.0	4.5	6.0	V	VIN=14V
	ON Threshold Voltage	VCEH	0.6	1.3	2.0	V	VIN=14V

Parameter		Symbol	Ratings			Unit	Test Condition
			MIN	TYP	MAX		
SYNC Terminal	Synchronous Threshold Voltage	VSYNC	-	1.85	-	V	VIN=14V, Vo=5V, IO=1A
	Synchronizing Frequency	FSYNC	300		1000	kHz	VIN=14V, Vo=5V, IO=1A
Thermal Shutdown Start Temperature		Tj	151	160		°C	
Error Amplifier Voltage Gain *5		AEA		800		V/V	
Error Amplifier Trans-conductance *5		GEA		800		uA/V	
Current Sense Amplifier Conductance*5		GCS		3.33		A/V	
Maximum ON Duty		DMAX		90		%	
Minimum ON Duty		DMIN		150		nsec	
High-side Switching ON resistance *5		RonH		150		mΩ	VIN=12V
Low-side Switching ON resistance *5		RonL		150		mΩ	VIN=12V

\*4: Efficiency should be calculated by using the following equation:  $\eta (\%) = \frac{V_o \cdot I_o}{V_{IN} \cdot I_{IN}} \times 100$

\*5: This is a design assurance value.

●2-3 Circuit Diagram

2-3-1 Internal Equivalent Circuit

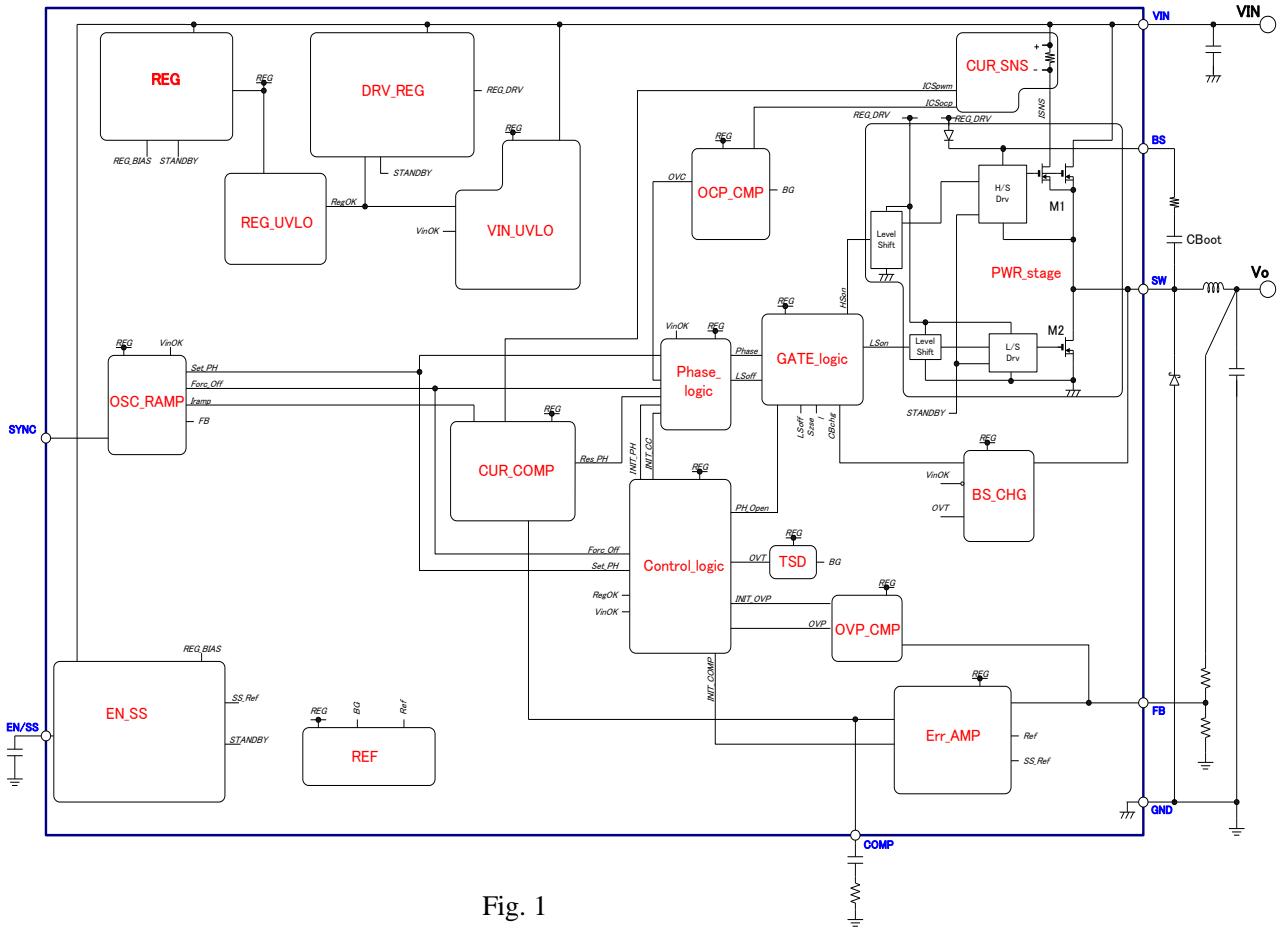
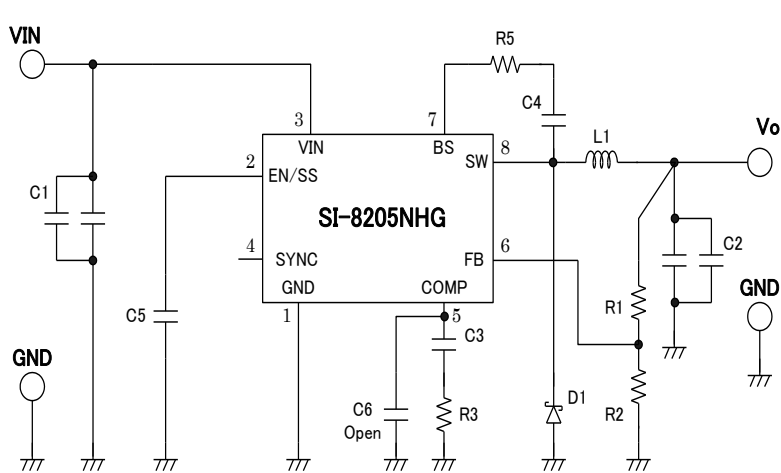


Fig. 1

2-3-2 Typical Connection Diagram



- C1:10 $\mu$ F/50V  $\times$  2
- C2:22 $\mu$ F/16V  $\times$  2
- C3:270pF
- C4:0.1 $\mu$ F
- C5:1 $\mu$ F
- A ceramics capacitor should be a good temperature character.
- L1:10 $\mu$ H
- D1: SJPB-L6 (SANKEN)
- R1:9k $\Omega$  (at Vo=5V)
- R2:1k $\Omega$
- R3:51k $\Omega$
- R5:20 $\Omega$  to 47 $\Omega$

Fig. 2

## 3. Terminal Description

### ●3-1 Terminal List

Table 4

Terminal	SI-8205NHG	
	Symbol	Description
1	GND	Ground Terminal
2	EN/SS	Soft Start Terminal (ON/OFF Terminal)
3	VIN	Input Terminal
4	SYNC	External Synchronization Signal Input Terminal
5	COMP	Phase Compensation Terminal
6	FB	Feedback Voltage Terminal
7	BS	High side Boost Terminal
8	SW	Switching Output Terminal

### ●3-2 Functional Description of Terminal

- GND (terminal No. 1)  
It is a ground terminal.
- EN/SS (terminal No. 2)  
It is a terminal for turning ON/OFF the IC. The soft start of output voltage can be made by connecting a capacitor to this terminal also.
- VIN (terminal No. 3)  
It is an input voltage of IC.
- SYNC (terminal No. 4)  
This pin is intended to operate the internal oscillator by external signals.
- COMP (terminal No. 5)  
It is a phase compensation terminal for controlling the loop stably.
- FB (terminal No. 6)  
It is a terminal for setting the output voltage. The output voltage is set by R1 and R2.
- BS (terminal No. 7)  
It is an internal power supply for driving the gate of high side switch Nch - MOS. A capacitor of 10 nF or more is connected between the SW terminal and BS terminal to drive the high side Nch - MOS.
- SW (terminal No. 8)  
It is a switching output terminal which supplies power to the output.





added signal does not exceed the COMP terminal voltage, the RS flip-flop is reset without fail by the signal of the 10% OFF Duty circuit.

#### ●4-2 Overcurrent Protection / Thermal Shutdown

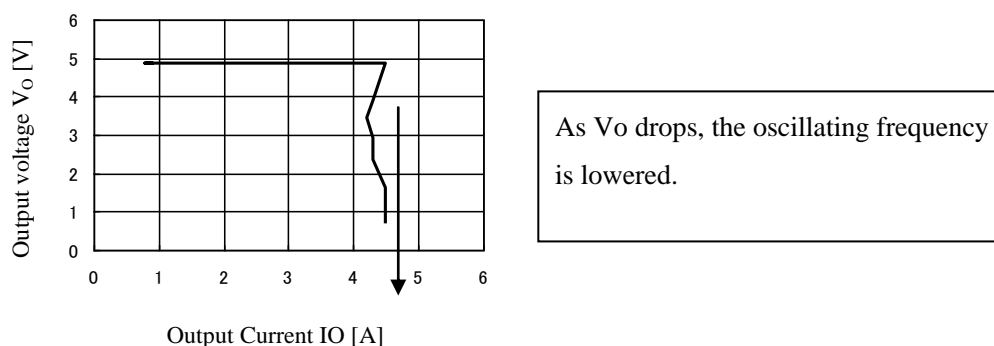


Fig.4 Output Voltage Characteristics in Overcurrent

The SI-8205NHG incorporates a current limiting type overcurrent protection circuit. The overcurrent protection circuit detects the peak current of a switching transistor and when the peak current exceeds the set value, the ON time of the transistor is compulsorily shortened to limit the current by lowering the output voltage. In addition, when the output voltage is lowered, the increase of current at low output voltage is prevented by dropping the switching frequency. When the overcurrent condition is released, the output voltage will be automatically restored.

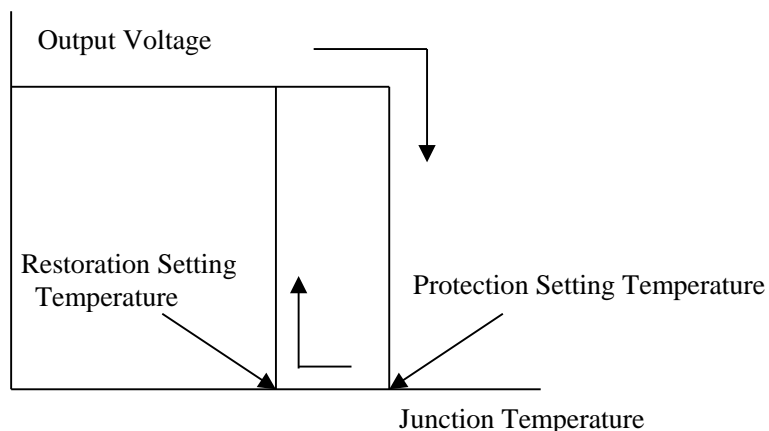


Fig.5 Output Voltage Characteristics in Thermal Shutdown

The thermal shutdown circuit detects the semiconductor junction temperature of the IC and when the junction temperature exceeds the set value (around 150°C), the output transistor is stopped and the output is turned OFF. When the junction temperature drops from the set value for overheat protection by around 10°C, the output transistor is automatically restored.

\* Note for thermal shutdown characteristic

This circuit protects the IC against overheat resulting from the instantaneous short circuit, but it should be noted that this function does not assure the operation including reliability in the state that overheat continues due to long time short circuit.

## 5. Cautions

### ●5-1 External Components

#### 5-1-1 Choke coil L1

The choke coil L1 plays a main role in the chopper type switching regulator. In order to maintain the stable operation of the regulator, such dangerous state of operation as saturation state and operation at high temperature due to heat generation must be avoided.

The following points should be taken into consideration for the selection of the choke coil.

a) The choke coil should be fit for the switching regulator.

The coil for a noise filter should not be used because of large loss and generated heat.

b) For the peak detection current control, the inductance current may fluctuate at the cycle of integral multiple of switching operation frequency.

Such phenomenon is called as sub harmonic oscillation and it may theoretically occur in the peak detection current control mode.

Therefore, in order to assure stable operation, the inductance current is compensated inside the IC, and it is required to select a proper inductance value to the output voltage.

Fig. 6 shows the selection range of the inductance L value to avoid the sub harmonic oscillation. The upper limit of inductance L is variable subject to the input/output conditions, load current etc., therefore please regard it as a reference in the Fig. 6 below.

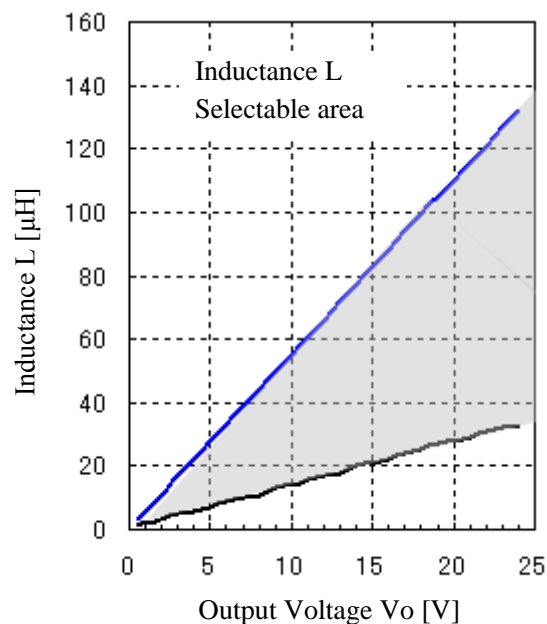


Fig. 6 Selection range of the inductance L value

The pulse current of choke coil  $\Delta IL$  and the peak current  $ILP$  are expressed by the following equation:

$$\Delta IL = \frac{(V_{in} - V_{out}) \cdot V_{out}}{L \cdot V_{in} \cdot f} \quad \text{--- (A)}$$

$$ILP = \frac{\Delta IL}{2} + I_{out} \quad \text{--- (B)}$$

From this equation, you will see that as the inductance  $L$  of choke coil is decreased,  $\Delta IL$  and  $ILP$  are increased. In the event that the inductance is too little, the fluctuation of choke coil current is larger, resulting in unstable operation of the regulator.

Care should be taken of decrease of inductance of choke coil due to magnetic saturation of overload, load short circuit etc.

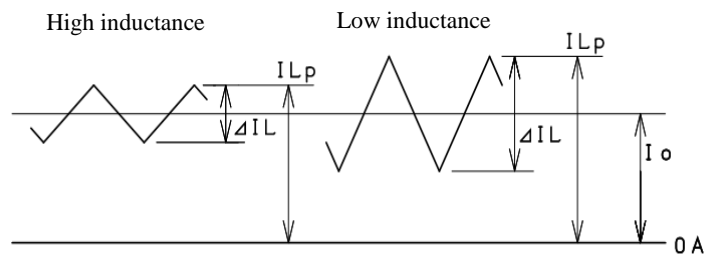


Fig.7 Relation between Ripple current  $ILP$  and Output Current  $I_O$

c) The rated current shall be met.

The rated current of the choke coil must be higher than the maximum load current to be used. When the load current exceeds the rated current of the coil, the inductance is sharply decreased to the extent that it causes saturation state at last. Please note that overcurrent may flow since the high frequency impedance becomes low.

d) Noise shall be low.

In the open magnetic circuit core which is of drum shape, since magnetic flux passes outside the coil, the peripheral circuit may be damaged by noise. It is recommended to use the toroidal type, EI type or EE type coil which has a closed magnetic circuit type core as much as possible.

### **5-1-2 Input Capacitor C1**

The input capacitor is operated as a bypass capacitor of the input circuit to supply steep current to the regulator during switching and to compensate the voltage drop of the input side. Therefore, the input capacitor should be placed as close as to the regulator IC.

Even in the case that the rectifying capacitor of the AC rectifier circuit is located in the input circuit, the input capacitor cannot play a role of the rectifying capacitor unless it is placed near the SI-8205NHG.

The selection of  $C1$  shall be made in consideration of the following points:

- a) The requirement of withstand voltage shall be met.
- b) The requirement of the allowable ripple voltage shall be met.

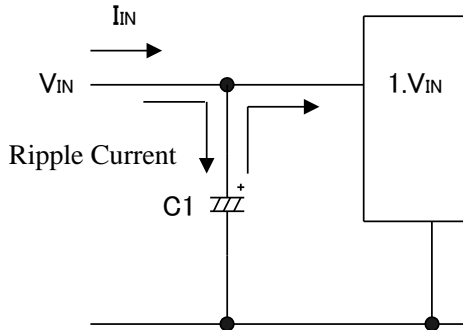


Fig.8 Current Flow of C1

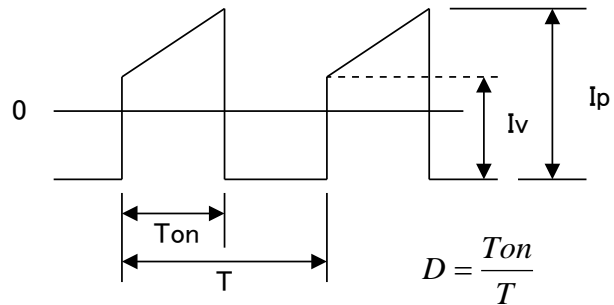


Fig. 9 Current Waveform of C1

The ripple current of the input capacitor is increased in accordance with the increase of the load current.

If the withstanding voltages or allowable ripple voltages are exceeded or used without derating, it is in danger of causing not only the decreasing the capacitor lifetime (burst, capacitance decrease, equivalent impedance increase, etc) but also the abnormal oscillations of regulator.

Therefore, the selection with sufficient margin is needed.

The effective value of ripple current flowing across the input capacitor can be obtained by the following equation (2):

$$I_{rms} \approx 1.2 \times \frac{V_o}{V_{in}} \times I_o \quad \text{--- (2)}$$

For instance, where  $V_{IN}=20V$ ,  $I_o=3A$ ,  $V_o=5V$

$$I_{r} \approx 1.2 \times \frac{5}{20} \times 3 = 0.9A$$

Therefore, it is necessary to select the capacitor with the allowable ripple current of 0.9A or higher.

### 5-1-3 Output Capacitor C2

The current control system is a voltage control system to which a loop which detects and feeds back the inductance current is added. By adding inductor current to the feedback loop, stable operation is realized without taking into consideration the influence of secondary delay of the LC filter. Therefore, the capacitance C of the LC filter which is required to compensate the secondary delay can be decreased and furthermore, stable operation can be obtained, even if the low ESR capacitor (ceramic capacitor) is used.

The output capacitor C2 composes a LC low pass filter together with a choke coil L1 and functions as a rectifying capacitor of switching output.

The current equivalent to the pulse current  $\Delta I_L$  of the choke coil current is charged and discharged in the

output capacitor.

Therefore, it is necessary to meet the requirements of withstand voltage and allowable ripple current with sufficient margin like the input capacitor.

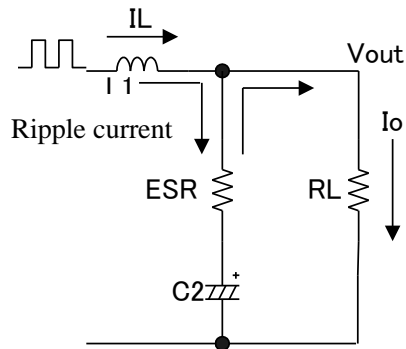
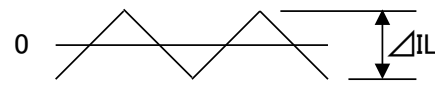


Fig.10 C2 current flow



The ripple current of the output capacitor is equal to the ripple current of the choke coil and does not vary even if the load current increases

Fig.11 C2 current curve

The ripple current effective value of the output capacitor is obtained by the equation (3).

$$I_{rms} = \frac{\Delta IL}{2\sqrt{3}} \quad \text{--- (3)}$$

When  $\Delta IL = 0.5A$ ,

$$I_{rms} = \frac{0.5}{2\sqrt{3}} \doteq 0.14A$$

Therefore a capacitor having the allowable ripple current of 0.14A or higher is required.

In addition, the output ripple voltage  $V_{rip}$  of the regulator is determined by a product of the pulse current  $\Delta IL$  of the choke coil current (= C2 charging/discharging current) and the equivalent series resistance ESR of the output capacitor.

$$V_{rip} = \Delta IL \cdot C2ESR \quad \text{--- (4)}$$

It is therefore necessary to select a capacitor with low equivalent series resistance ESR in order to lower the output ripple voltage. As for general electrolytic capacitors of same product series, the ESR shall be lower, for the products of higher capacitance with same withstand voltage, or with higher withstand voltage (almost proportional to larger externals) with same capacitance.

When  $\Delta IL=0.5A$ ,  $V_{rip}=40mV$ ,

$$C2esr = 40 \div 0.5 = 80m\Omega$$

As shown above, a capacitor with the ESR of 80mΩ or lower should be selected. In addition, since the ESR varies with temperature and increases at low temperature, it is required to examine the ESR at the actual operating temperatures. It is recommended to contact capacitor manufacturers for the ESR value since it is peculiar to capacitors.

#### **5-1-4 Flywheel Diode D1**

The SI-8205NHG has a switch-over function between synchronous rectification and asynchronous one subject to input/output conditions, load conditions etc.. Since asynchronous operation is made as well, it is recommended to connect a fly wheel diode D1 externally.

The flywheel diode D1 is to discharge the energy which is stored in the choke coil at switching OFF.

For the flywheel diode, the Schottky barrier diode must be used. If a general rectifying diode or fast recovery diode is used, the IC may be destroyed by applying reverse voltage due to the recovery and ON voltage.

In addition, since the output voltage from the SW terminal (pin 8) of the SI-8205NHG series is almost equivalent to the input voltage, the flywheel diode with the reverse withstand voltage of the input voltage or higher should be used.

It is recommended not to use the ferrite bead for the flywheel diode.

#### **5-1-5 Phase compensation elements C3, C6, R3**

The stability and responsiveness of the loop are controlled through the COMP terminal.

The COMP terminal is an output of the internal trans-conductance amplifier.

The series combination of a capacitor and resistor sets the combination of pole and zero which determines characteristics of the control system. The DC gain of voltage feedback loop can be calculated by the following equation:

$$A_{dc} = R_l \times G_{cs} \times A_{EA} \times \frac{V_{FB}}{V_{out}}$$

Here,  $V_{FB}$  is feedback voltage (0.5V).  $A_{EA}$  is the voltage gain of error amplifier,  $G_{CS}$  trans-inductance of current detection and  $R_l$  a load resistance value. There are two important poles. One is produced by a phase compensation capacitor (C3) and an output resistor of the error amplifier.

Another one is produced by a output capacitor and a load resistor. These poles appear at the following frequencies:

$$fp1 = \frac{G_{EA}}{2\pi \times C3 \times A_{EA}}$$

$$fp2 = \frac{1}{2\pi \times C2 \times R_l}$$

Here,  $G_{EA}$  is the trans-conductance of error amplifier. In this system, one zero is important. This zero is produced by phase compensation capacitor C3 and phase compensation resistance R3. This zero appears in the following frequencies:

$$fz1 = \frac{1}{2\pi \times C3 \times R3}$$

If the output capacitor is large and/or ESR is large, this system may have another important zero. This zero is produced by the ESR and capacitance of the output capacitor. And it exists in the following frequencies:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times RESR}$$

In this case, the third pole which is set by the phase compensation capacitor (C6) and phase compensation resistor (R3) is used to compensate the effect of ESR zero on the loop gain.

This pole exists in the following frequencies:

$$fp3 = \frac{1}{2\pi \times C6 \times R3}$$

The objective of design of phase compensation is to form the converter transfer function to obtain the desired loop gain. The system crossover frequency where the feedback loop has a single gain is important. The lower crossover frequency will produce the slower line and load transient. In the meantime, the higher crossover frequency may cause instability of the system. The selection of the most suitable phase compensation element is described below.

1. A phase compensation resistor (R3) is selected to set the resistor at the desired crossover frequency.

The calculation of R3 is made by the following equation:

$$R3 = \frac{2\pi \times C2 \times fc}{GEA \times GCS} \times \frac{Vout}{VFB} < \frac{2\pi \times C2 \times 0.1 \times fs}{GEA \times GCS} \times \frac{Vout}{VFB}$$

Here, fc is a desired crossover frequency. It should be one tenth or lower of the normal switching frequency (fs).

2. In order to achieve the desired phase margin, a phase compensation capacitor (C3) is selected.

For the application having a representative inductance value, adequate phase margin is provided by setting the zero compensation of one fourth or lower of the crossover frequency.

C3 is calculated by the following equation.

$$C3 > \frac{4}{2\pi \times R3 \times fc}$$

R3 is a phase compensation resistor.

3. It is required to judge whether the second compensation capacitor C6 is necessary or not.

It will be necessary, when the ESR zero of the output capacitor is located at a frequency which is lower than the half of the switching frequency.

Namely, it is necessary, when the following equation is applicable.

$$\frac{1}{2\pi \times C2 \times RESR} < \frac{fs}{2}$$

In this case, the second compensation capacitor C6 is added and the frequency fp3 of ESR zero is set.

C6 is obtained from the following equation.

$$C6 = \frac{C2 \times RESR}{R3}$$

The constants for each output setting voltage in the case that ceramic capacitors or aluminum electrolytic capacitors are used are shown in the following table.

The inductor L should be selected by reference to the choke coil L1 of 5-1-1. (Refer to Fig. 6 Scope of



selection of inductance L value)

Vout [V]	L [uH]	Cout[uF] (ceramic capacitor)	fc=50kHz			fc=20kHz		
			R3 [kΩ]	C3 [pF]	C6 [pF]	R3 [kΩ]	C3 [pF]	C6 [pF]
1.2	2.0 - 10	22 x 2	12	1000	No	4.7	6800	No
1.8	3.0 - 10	22 x 2	18	680	No	7.3	4700	No
3.3	6.8 - 16	22 x 2	33	330	No	13	3300	No
5	8.2 - 22	22 x 2	51	220	No	20	1800	No
12	22 - 68	22 x 2	124	100	No	47	680	No

Table 5  
Output  
setting  
voltage (use  
ceramic  
capacitors)

Vout [V]	L [uH]	Cout [uF]/ ESR [mΩ] (aluminum electrolytic capacitor)	fc=50kHz			fc=20kHz		
			R3 [kΩ]	C3 [pF]	C6 [pF]	R3 [kΩ]	C3 [pF]	C6 [pF]
1.2	2.0 - 10	220/100	62	220	470	24	1500	1000
1.8	3.0 - 10	220/100	91	180	330	36	1000	680
3.3	6.8 - 16	220/100	160	100	180	68	470	330
5	8.2 - 22	220/100	240	100	100	100	330	220
12	22 - 68	220/100	620	100	100	240	150	100

Table 6 Output setting voltage (use aluminum electrolytic capacitors)

## ●5-2 Pattern Design Notes

### 5-2-1 High Current Line

Since high current flows in the bold lines in the connection diagram, the pattern should be as wide and short as possible.

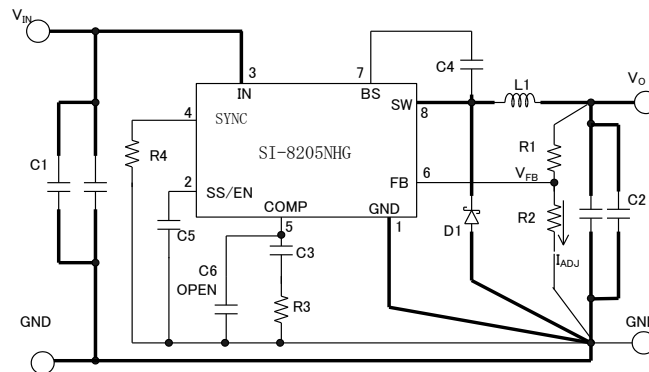


Fig. 12 Circuit Diagram

### 5-2-2 Input/ Output Capacitor

The input capacitor C1 and the output capacitor C2 should be placed to the IC as close as possible. If the rectifying capacitor for AC rectifier circuit is on the input side, it can be used as an input capacitor. However, if it is not close to the IC, the input capacitor should be connected in addition to the rectifying capacitor. Since high current is discharged and charged through the leads of input/output capacitor at high speed, the leads should be as short as possible. A similar care should be taken for the patterning of the capacitor.

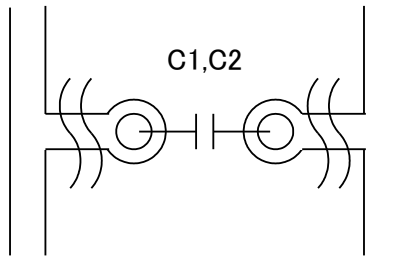


Fig. 13 Improper Pattern Example

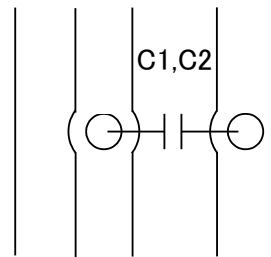


Fig. 14 Proper Pattern Example

### 5-2-3 FB Terminal (Output Voltage Set-up)

The FB terminal is a feedback detection terminal for controlling the output voltage. It is recommended to connect it as close as possible to the output capacitor C2. When they are not close, the abnormal oscillation may be caused due to the poor regulation and increase of switching ripple. The output voltage set-up is achieved by connecting R1 and R2.  $I_{FB}$  should be set to be around 0.5mA.

(The  $I_{FB}$  lower limit is 0.5mA, and the upper limit is not defined. However, it is necessary to consider that the consumption current shall increase according to the  $I_{FB}$  value, resulting in lower efficiency.)

R1, R2 and output voltage are calculated from the following equations:

$$I_{FB} = V_{FB} / R2 \quad *V_{FB} = 0.5V \pm 1\%$$

$$R1 = (V_o - V_{FB}) / I_{FB} \quad R2 = V_{FB} / I_{FB}$$

$$V_{out} = R1 \times (V_{FB} / R2) + V_{FB}$$

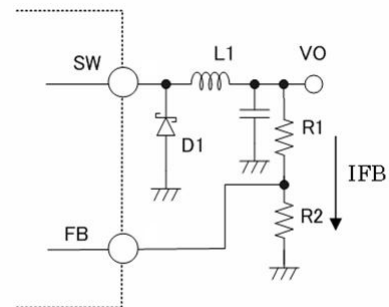


Fig. 15

- R2 should be connected for the stable operation when set to  $V_o = 0.5V$ .
- As to the relationship with the input/output voltage, it is recommended to set the ON width of SW terminal to be 200 nsec or longer.

The wiring of COMP terminal, FB terminal, R1 and R2 that run parallel to the flywheel diode should be avoided, because switching noise may interfere with the detection voltage to cause abnormal oscillation. It is recommended to implement the wiring from the FB terminal to R2 as short as possible.

- Mounting Board Pattern Example  
Surface Mounting Type (SI-8205NHG)

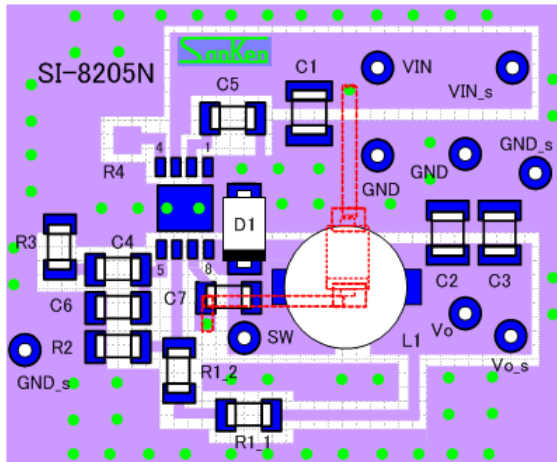


Fig. 16 Front side: materials on this side

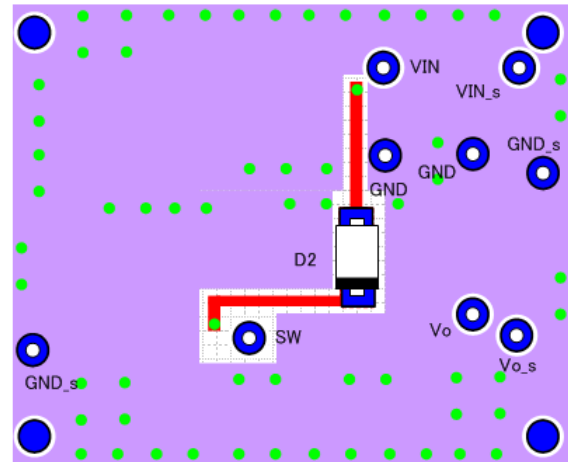


Fig. 17 Back side: GND side

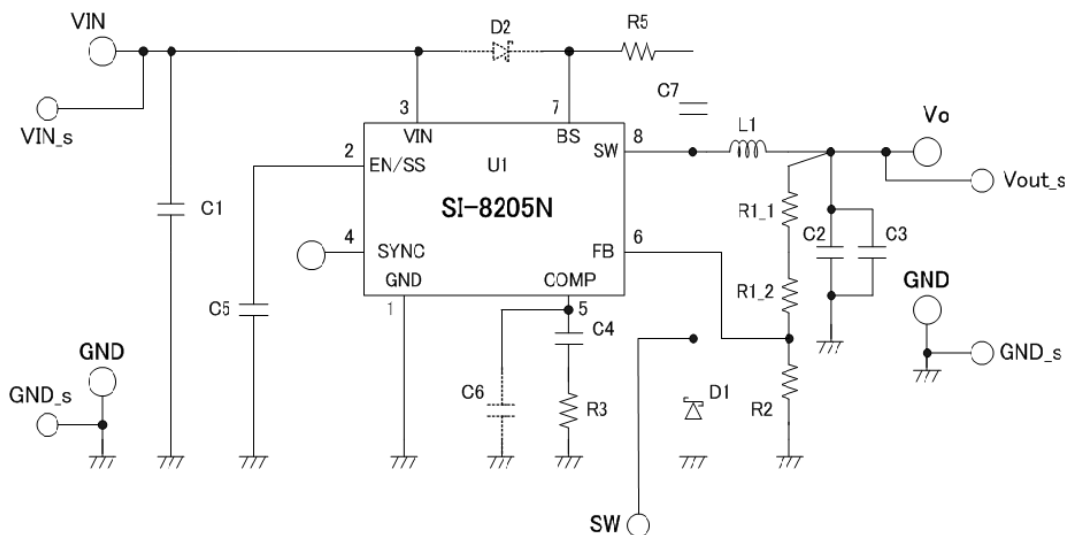


Fig. 18 Pattern Circuit Diagram

### 5-3 Power Supply Stability

The phase characteristics of the chopper type regulator are synthesized by the phase characteristics inside the regulator IC and that of output capacitor  $C_{out}$  and the load resistor  $R_{out}$ . The phase characteristics inside the regulator IC are generally determined by the delay time of the control block and the phase characteristic of the output error amplifier. Among these two factors, the phase delay due to the delay time of the control block rarely causes problems in actual use. Therefore, the phase characteristics of the error amplifier are important. With respect to the compensation of phase characteristics of the output error amplifier, external parts such as resistors and capacitors should be connected outside the IC for phase compensation.

Please refer to phase compensation elements C3, C6 and R3 of 5-1-5.

## 6. Applications

### ●6-1 Soft Start

When a capacitor is connected to terminal 2, the soft start is activated when the input voltage is applied.

$V_{out}$  rises in relation with the charging voltage of  $C_{ss}$ . Therefore, the rough estimation is done by the time constant calculation of  $C_{ss}$  charging.

The capacitor  $C_{ss}$  controls the rise time by controlling the OFF period of PWM control. The rise time  $t_{ss}$  and the delay time  $t_{delay}$  are obtained approximately by the following equation:

It is the delay time  $t_{delay}$  when voltage of EN/SS terminal  $< 1.6V$ .

It is the rise time  $t_{ss}$  when  $1.6V < \text{voltage of EN/SS} < 2.1V$

$$t_{delay} = C_{EN/SS} \times V_{EN/SS-1} / I_{EN/SS} = 0.1\mu F \times 1.6V / 5\mu A = 32msec$$

$$t_{ss} = C_{EN/SS} \times (V_{EN/SS-2} - V_{EN/SS-1}) / I_{EN/SS} = 0.1\mu F \times 0.5V / 5\mu A = 10msec$$

When not using the soft start function, the No.2 terminal should be open.

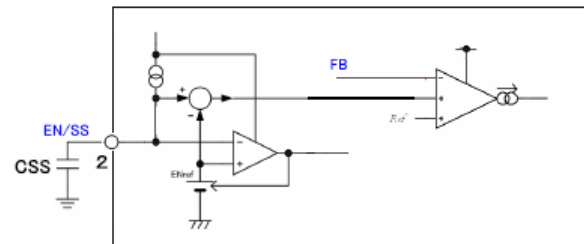
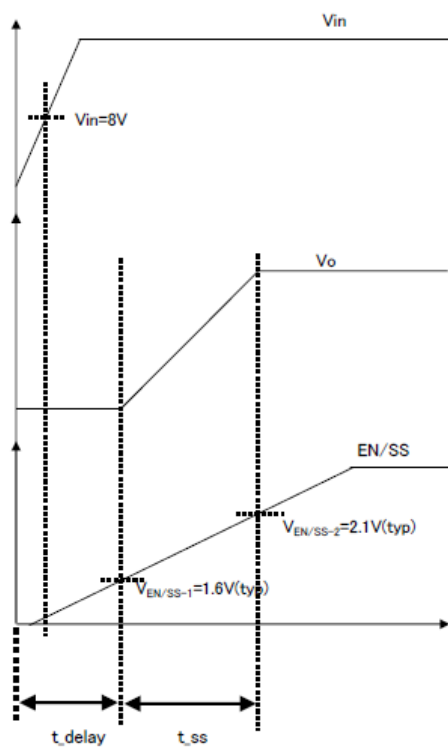


Fig. 19 Characteristic on Soft Start

Since the EN/SS terminal is pulled up (4.5V TYP) with the internal power supply of IC, the external voltage can not be applied.

If there is no  $C_{ss}$  or it is extremely low,  $V_{out}$  rises at the time constants charging the output capacitor with the output current restricted by the overcurrent protection  $I_s$ .

Time constants at output capacitor start-up

$$t = (C_o \times V_o) / I_s \text{ (at no load)}$$

\*The amount of load current is deducted from the Is value at load.

### ●6-2 Output ON / OFF Control

The output ON-Off control is possible using the EN/SS terminal (No.2). The output is turned OFF when the terminal 5 voltage falls below  $V_{C/EH}$  (1.6V TYP) by such as open collector. It is possible to use the soft start together. Since the soft start terminal has been already pulled up (4.5V TYP), no voltage shall be applied from the external side.

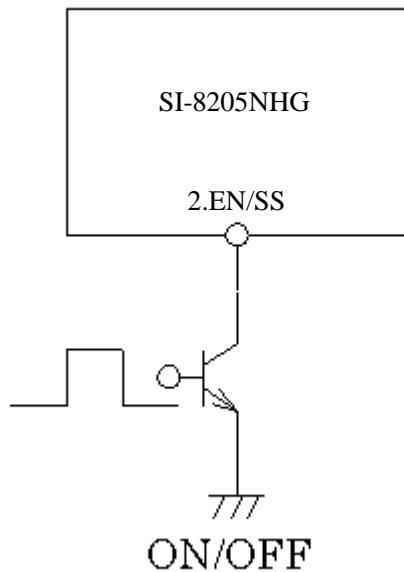


Fig. 20 ON / OFF Control 1

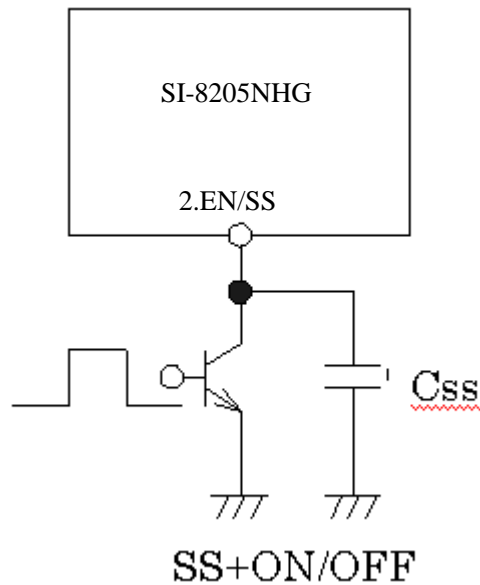


Fig. 21 ON / OFF Control 2

### ●6-3 Spike Noise Reduction

In order to reduce the spike noise, it is possible to compensate the output waveform of the SI-8205NHG and the recovery time of the diode by a capacitor (snubber), but it should be noted that the efficiency is also slightly reduced.

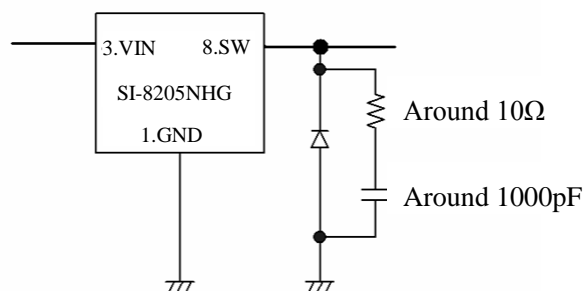


Fig. 22 Example of Snubber

\* When the spike noise is observed with an oscilloscope, the lead wire may function as an antenna and the spike noise may be observed extremely higher than usual if the probe GND lead wire is too long. In the observation of spike noise, the probe lead wire should be as short as possible and be connected with the root of the output capacitor.

#### ●6-4 Reverse Bias Protection

A diode for reverse bias protection will be required between input and output when the output voltage is higher than the input terminal voltage, such as in battery chargers.

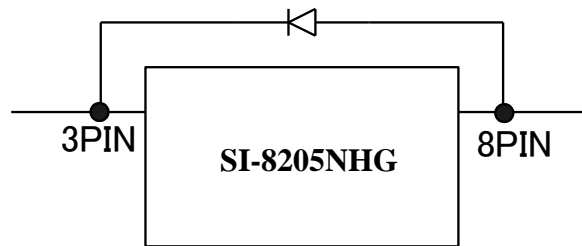


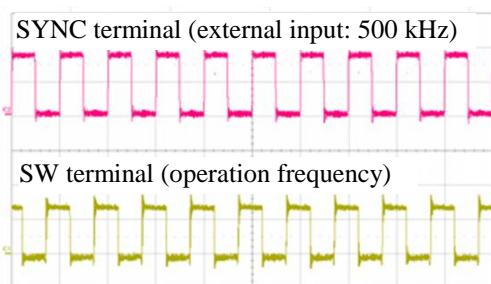
Fig. 23 Diode for Reverse Bias Protection

#### ●6-5 External synchronization

When the external signal is input (300kHz (TYP) to 1MHz (TYP)) to the 4th pin, operation can be performed at a frequency in synchronization with external signals. Fig.24 shows the operating waveform in synchronization with external signals. In addition, the operation is performed at a fixed frequency 250kHz by connecting the 4th pin to GND.

**Condition** :  $V_{IN} = 7V$   $V_O = 3.3V$   $I_O = 1A$

**External synchronization 500 kHz (2  $\mu$ sec/ div)**



**External synchronization 1 MHz (1  $\mu$ sec/ div)**

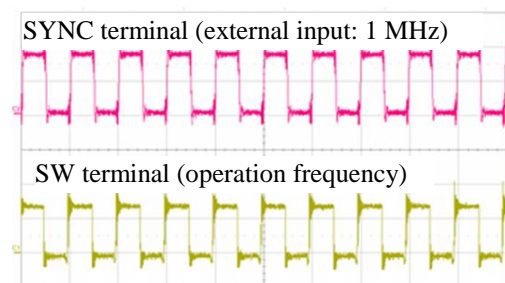


Fig.24 External synchronization operation

## 7. Terminology

- Jitter

It is a kind of abnormal switching operations and is a phenomenon that the switching pulse width varies in spite of the constant condition of input and output. The output ripple voltage peak width is increased when a jitter occurs.

- Recommended Conditions

It shows the operation conditions required for maintaining normal circuit functions. It is required to meet the conditions in actual operations.

- Absolute Maximum Ratings

It shows the destruction limits. It is required to take care so that even one item does not exceed the specified value for a moment during instantaneous or normal operation.

- Electrical Characteristics

It is the specified characteristic value in the operation under the conditions shown in each item. If the operating conditions are different, it may be out of the specifications.

- PWM (Pulse Width Modulation)

It is a kind of pulse modulation systems. The modulation is achieved by changing the pulse width in accordance with the variation of modulation signal waveform (the output voltage for chopper type switching regulator).

- ESR (Equivalent Series Resistance)

It is the equivalent series resistance of a capacitor. It acts in a similar manner to the resistor series-connected to the capacitor.



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