

## N-channel 600 V, 0.168 $\Omega$ typ., 17 A MDmesh™ II Power MOSFET in a D<sup>2</sup>PAK package

Datasheet – production data

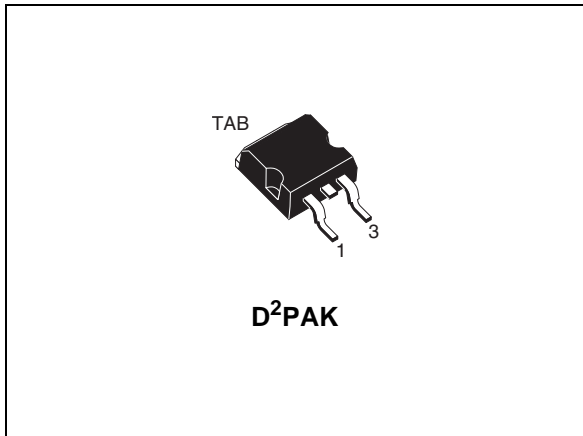
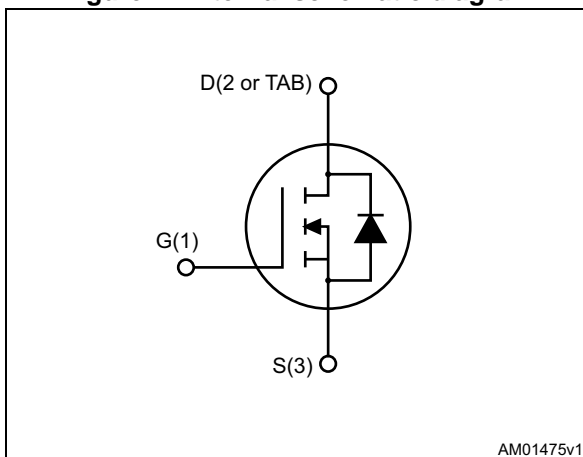


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub> @T <sub>jmax</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB24NM60N	650 V	0.19 $\Omega$	17 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STB24NM60N	24NM60N	D <sup>2</sup> PAK	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11	A
$I_{DM}^{(1)}$	Drain current (pulsed)	68	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 17\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ , peak  $V_{DS} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	1	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	30	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 oz Cu

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	300	mJ

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0, I <sub>D</sub> = 1 mA	600			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0, V <sub>DS</sub> = 600 V			1	μA
		V <sub>GS</sub> = 0, V <sub>DS</sub> = 600 V, T <sub>C</sub> = 125 °C			100	μA
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0, V <sub>GS</sub> = ± 25 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static drain-source on- resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8 A		0.168	0.19	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	1330	-	pF
C <sub>oss</sub>	Output capacitance		-	80	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	3.2	-	pF
C <sub>oss eq.</sub> <sup>(1)</sup>	Equivalent output capacitance	V <sub>DS</sub> = 0 to 480 V, V <sub>GS</sub> = 0	-	182	-	pF
R <sub>g</sub>	Gate input resistance	f = 1 MHz open drain	-	5	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 17 A, V <sub>GS</sub> = 10 V (see Figure 15)	-	44	-	nC
Q <sub>gs</sub>	Gate-source charge		-	7	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	24	-	nC

1. C<sub>o(eff)</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DS</sub>.

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 8.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 14)	-	11.5	-	ns
$t_{r(v)}$	Voltage rise time		-	16.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	73	-	ns
$t_{f(i)}$	Fall time		-	37	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 16)	-	340		ns
$Q_{rr}$	Reverse recovery charge		-	4.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	27		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16)	-	404		ns
$Q_{rr}$	Reverse recovery charge		-	5.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	28		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

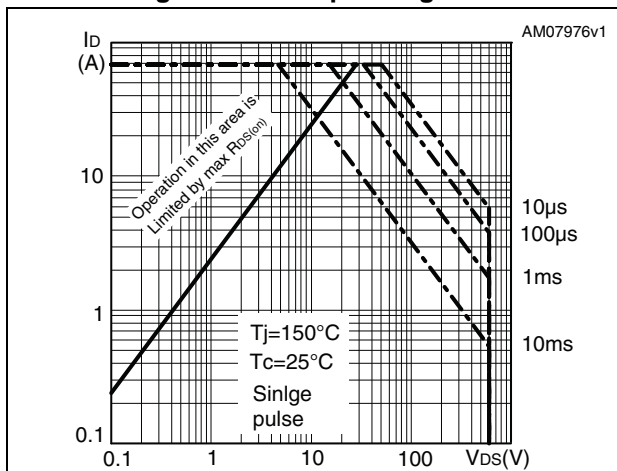


Figure 3. Thermal impedance

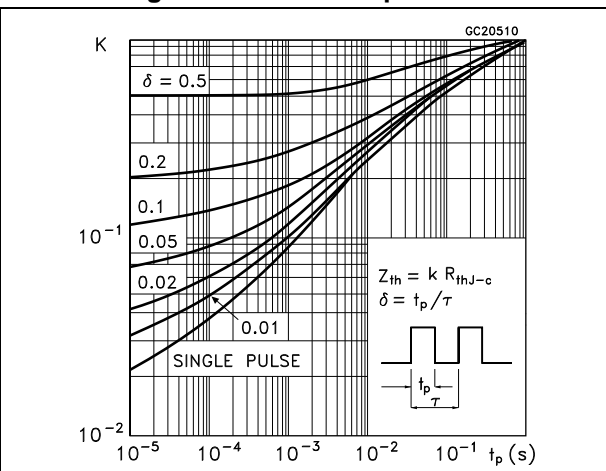


Figure 4. Output characteristics

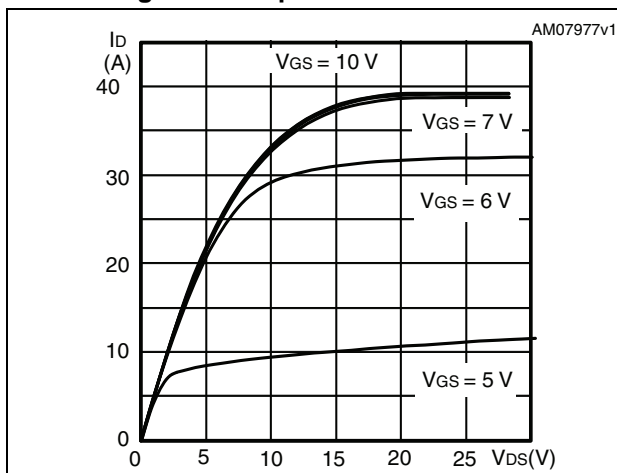


Figure 5. Transfer characteristics

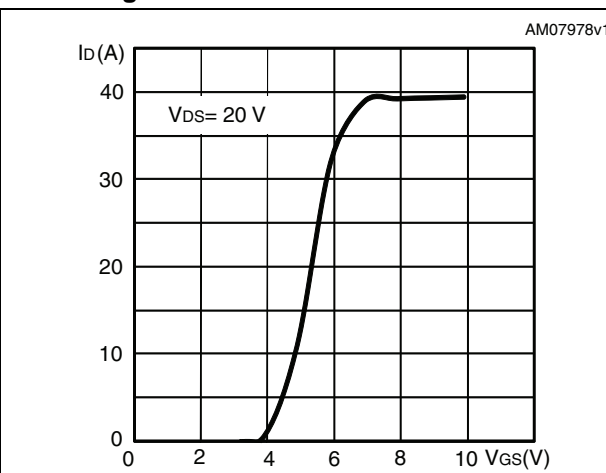


Figure 6. Gate charge vs gate-source voltage

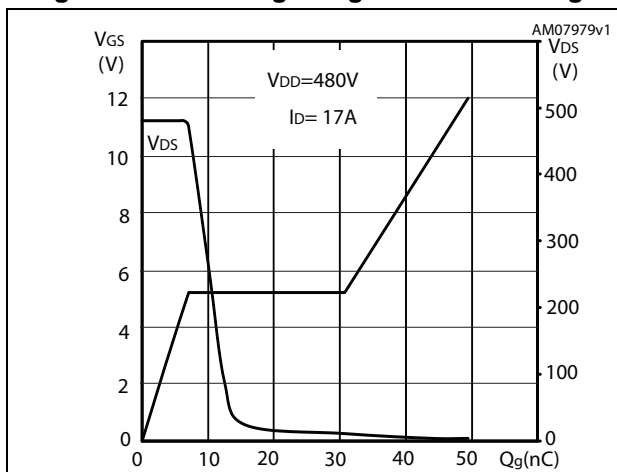


Figure 7. Static drain-source on-resistance

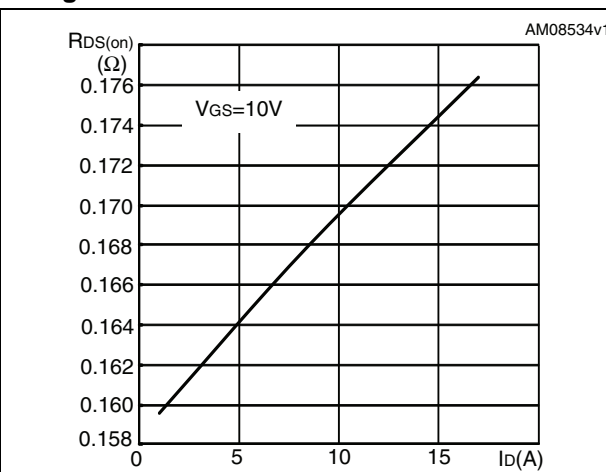


Figure 8. Capacitance variations

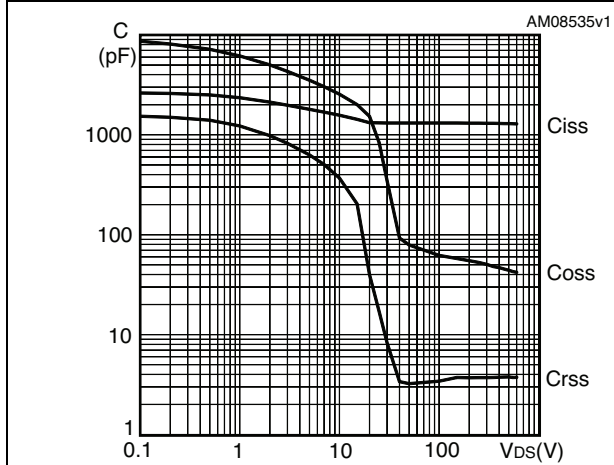


Figure 9. Output capacitance stored energy

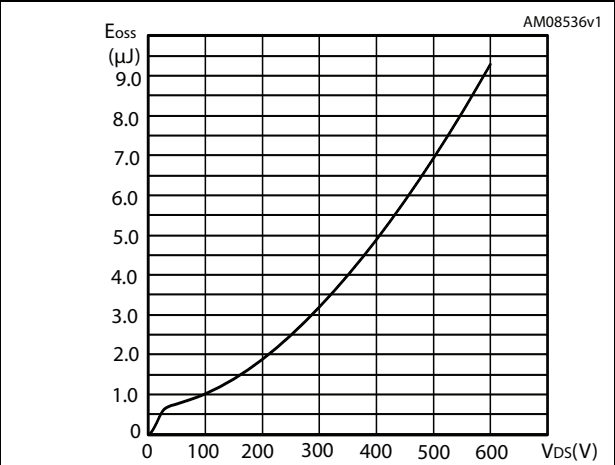


Figure 10. Normalized gate threshold voltage vs temperature

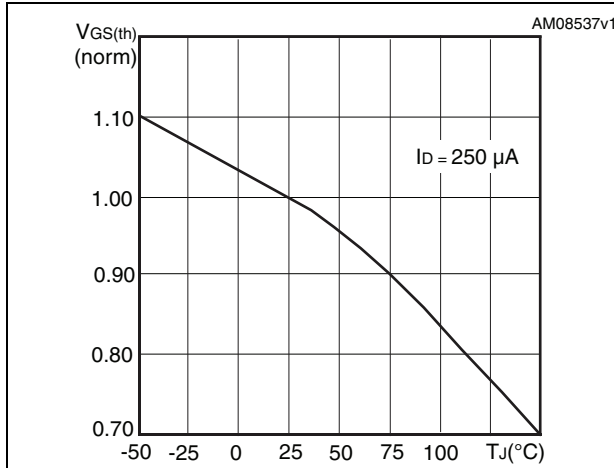


Figure 11. Normalized on-resistance vs temperature

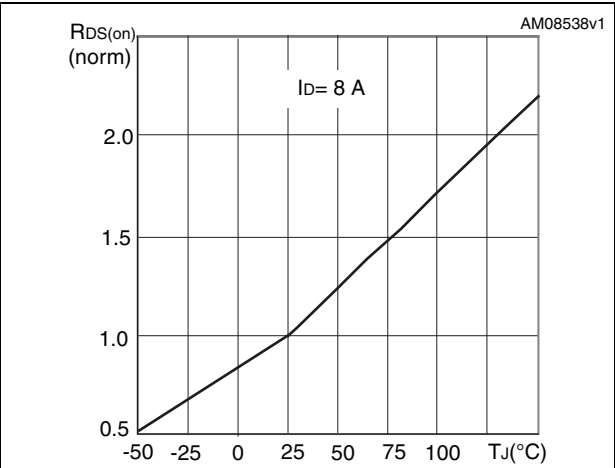


Figure 12. Normalized V(BR)DSS vs temperature

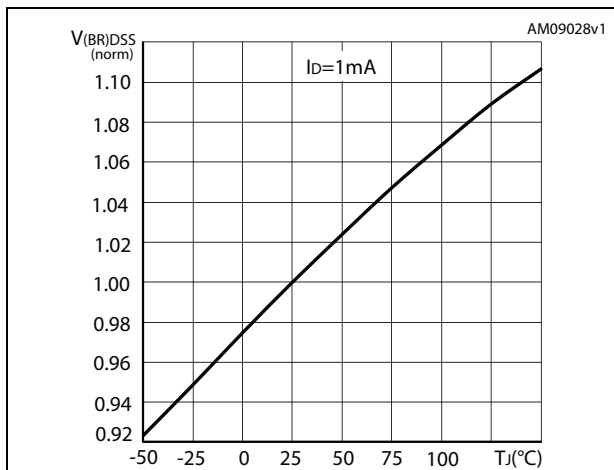
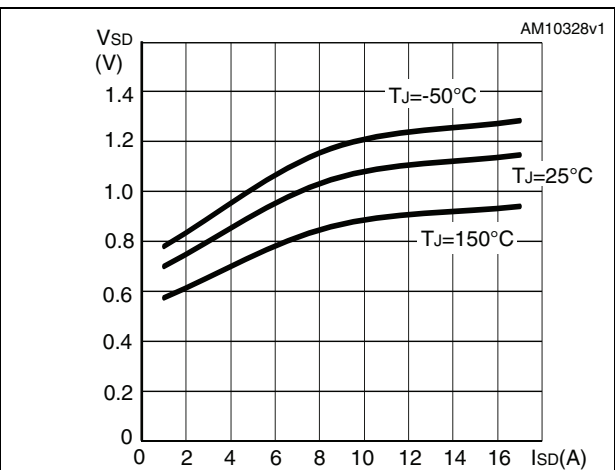


Figure 13. Source-drain diode forward characteristics



### 3 Test circuits

Figure 14. Switching times test circuit for resistive load



Figure 15. Gate charge test circuit



Figure 16. Test circuit for inductive load switching and diode recovery times



Figure 17. Unclamped inductive load test circuit



Figure 18. Unclamped inductive waveform



Figure 19. Switching time waveform





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 20. D<sup>2</sup>PAK (TO-263) drawing

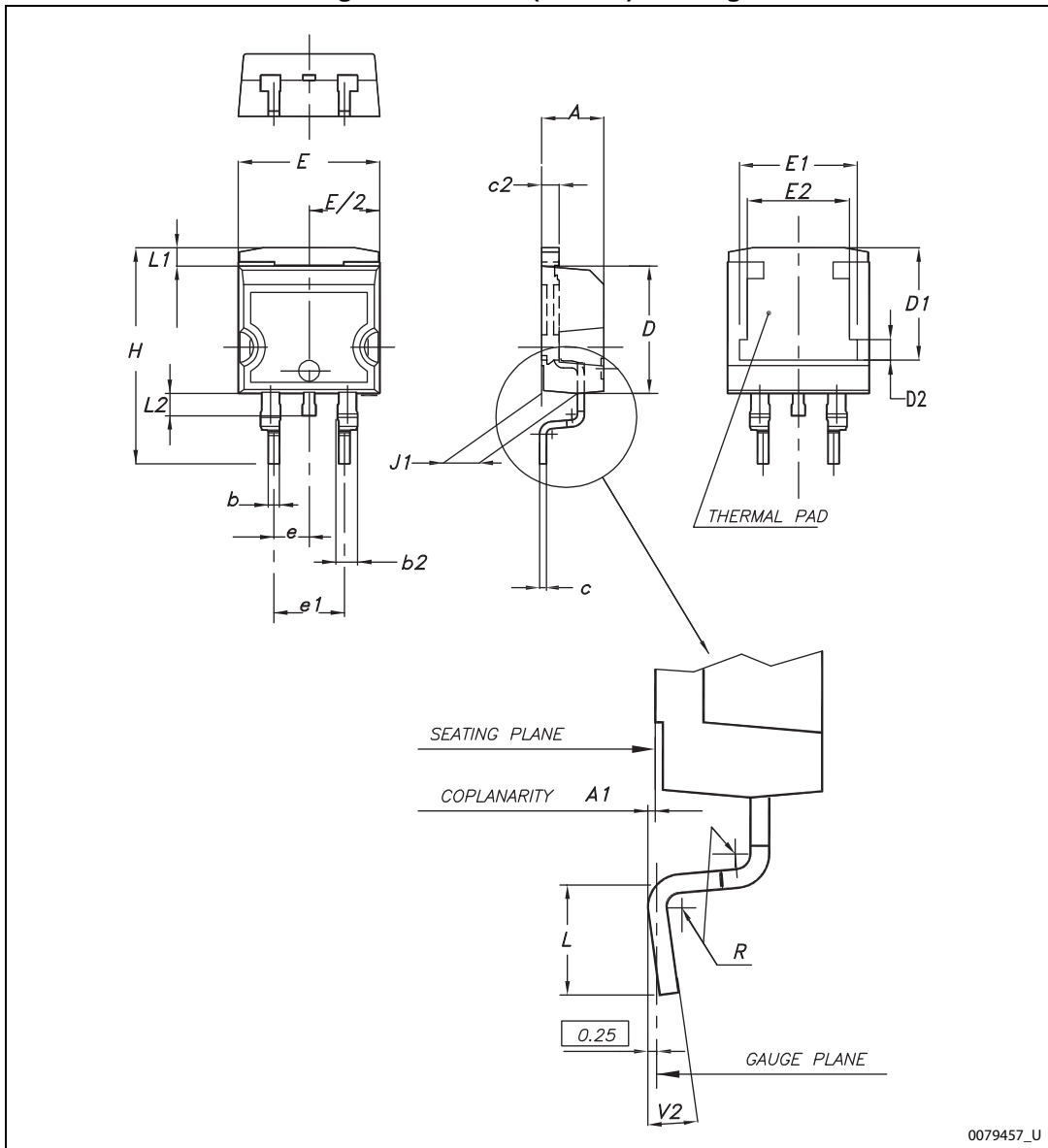
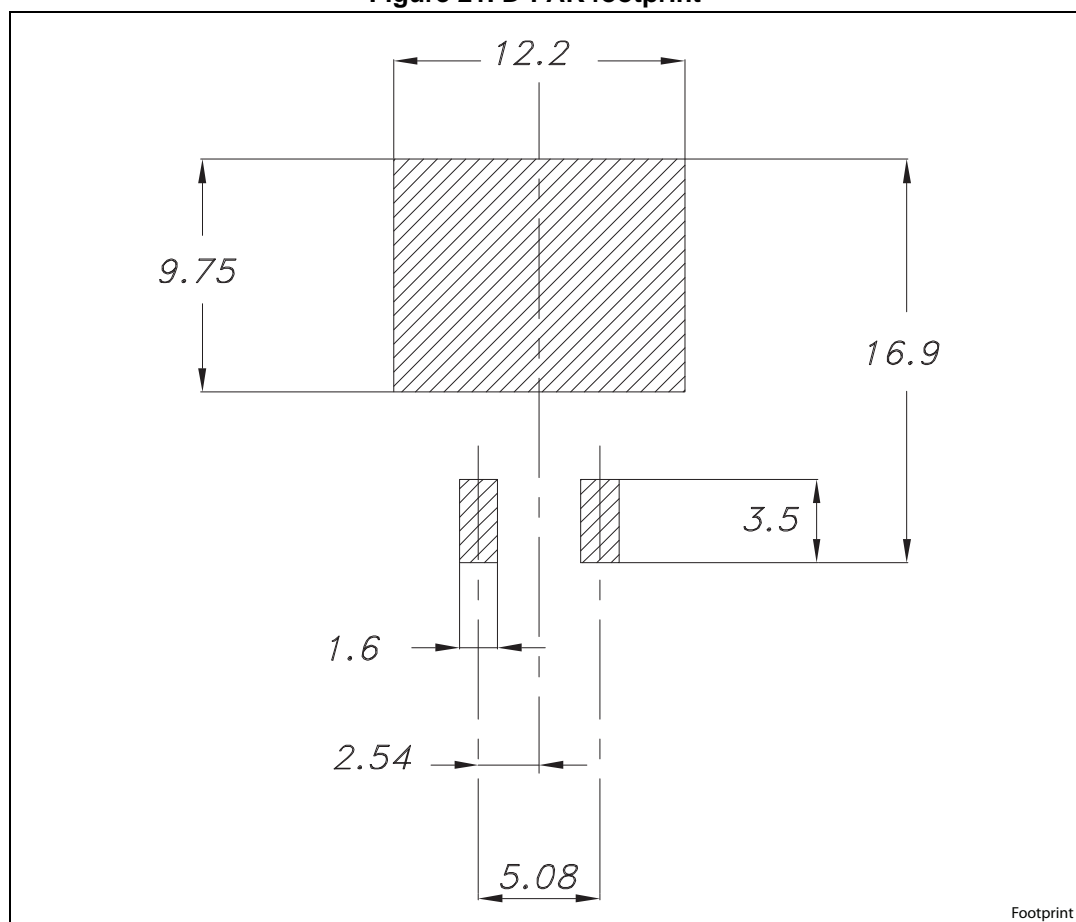


Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 21. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
05-Jan-2011	1	First release.
24-Jul-2014	2	<ul style="list-style-type: none"><li>– Modified: the entire typical values in <a href="#">Table 6</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>

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