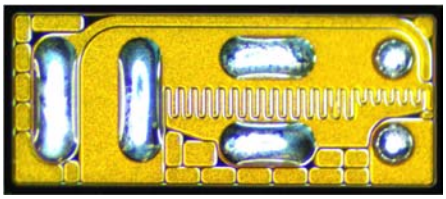
EPC8005 – Enhancement Mode Power Transistor
Preliminary Specification Sheet

Features:

- V_{DS}, 65V
- $R_{DS(on)}$, 275 mΩ
- I_D, 2.9 A
- Optimized eGaN® FET for high frequency applications
- Pb-Free (RoHS Compliant), Halogen Free



EPC8005 eGaN FETs are supplied only in passivated die form with solder bars

Applications:

- Ultra high speed DC-DC conversion
- RF Envelope Tracking
- Wireless Power Transfer
- Game console and industrial movement sensing (LiDAR)

MAXIMUM RATINGS

Parameter	Value
Maximum Drain – Source Voltage	65 V
Gate – Source Maximum Voltage Range	-5 V < V_{GS} < 6 V
Continuous Drain Current, 25 ˚C, θ_{JA} = 33	2.9 A
Maximum Pulsed Drain Current, 25 ˚C, T_{pulse} = 300 µs	3.8 A
Operating Temperature Range	-40 ˚C < T_J < 150 ˚C

STATIC CHARACTERISTICS

Parameter	Conditions	Value
Maximum Drain – Source Leakage	V_{DS} = 52 V, V_{GS} = 0 V	0.1 mA
Maximum $R_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.5 A	275 mΩ
Gate – Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.25 mA	0.7 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	V_{GS} = 5 V	0.5 mA
Gate – Source Maximum Negative Leakage	V_{GS} = -5 V	-0.1 mA

T_J = 25 °C unless otherwise stated
Specifications are with Substrate shorted to Source where applicable

DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value
C_{ISS} (Input Capacitance)	V_{DS} = 32.5 V; V_{GS} = 0 V	29 pF
C_{OSS} (Output Capacitance)		9.7 pF
C_{RSS} (Reverse Transfer Capacitance)		0.2 pF
Q_G (Total Gate Charge)	V_{DS} = 32.5 V; I_D = 1 A	218 pC
Q_{GD} (Gate to Drain Charge)		18 pC
Q_{GS} (Gate to Source Charge)		77 pC
Q_{OSS} (Output Charge)	V_{DS} = 32.5 V; V_{GS} = 0 V	414 pC
Q_{RR} (Source-Drain Recovery Charge)		0 pC

T_J = 25 °C unless otherwise stated
Specifications are with Substrate shorted to Source where applicable

THERMAL CHARACTERISTICS

		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.7	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	33	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	82	°C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Figure 1:

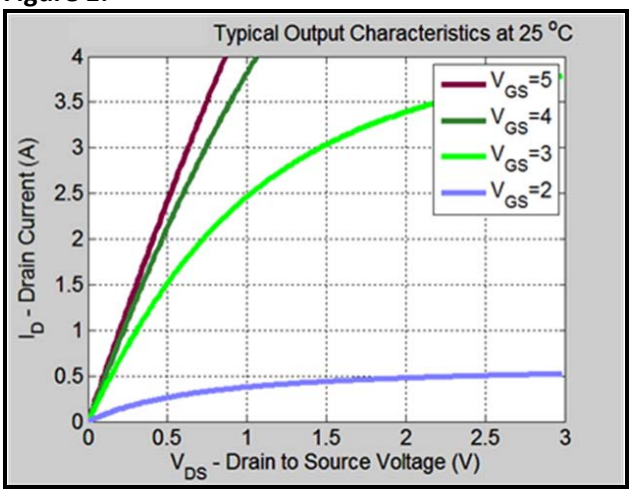


Figure 2:

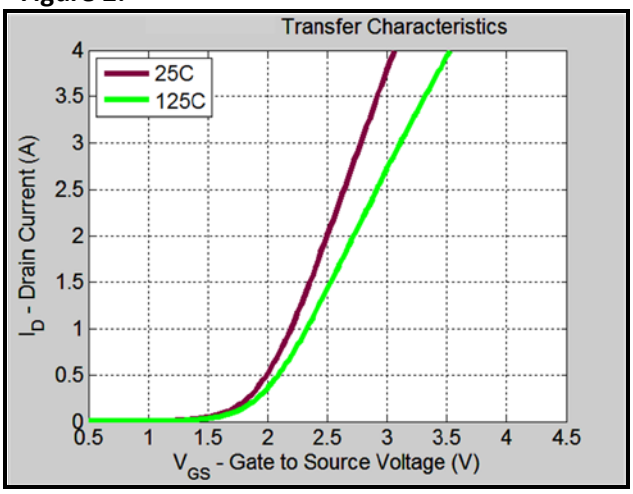


Figure 3:

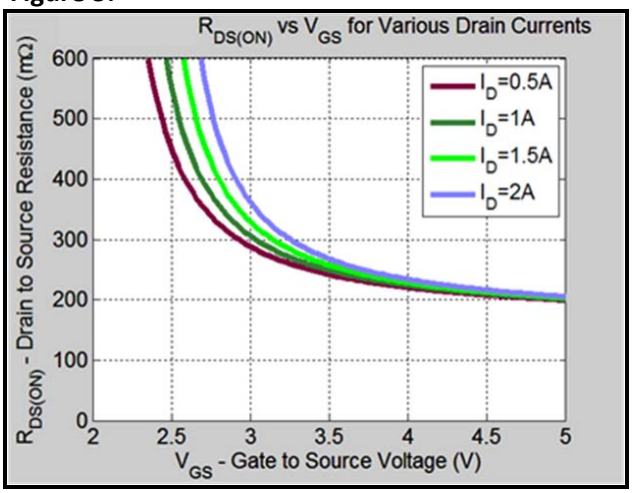


Figure 4:

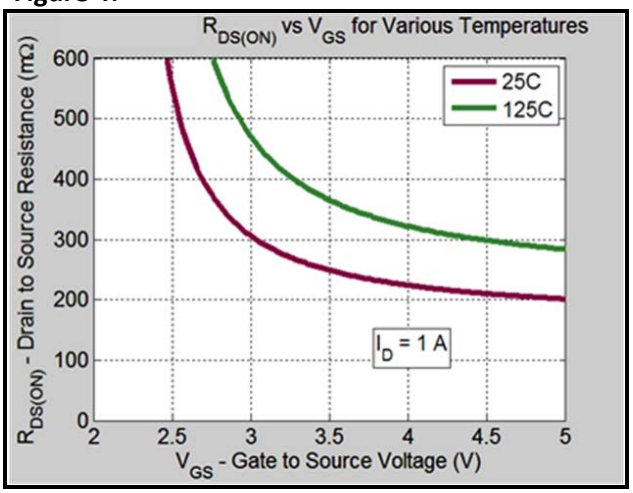
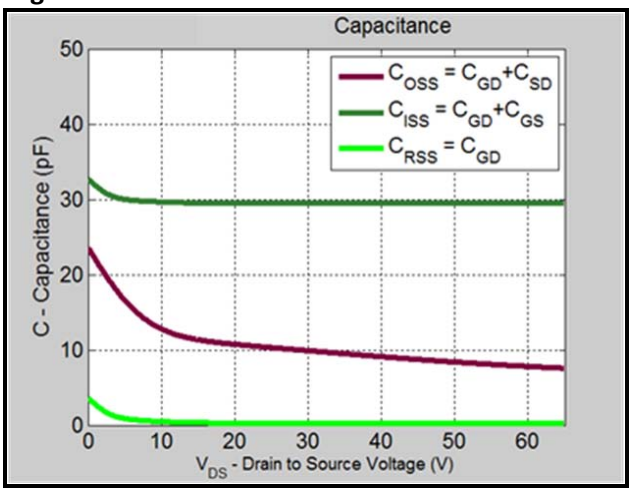
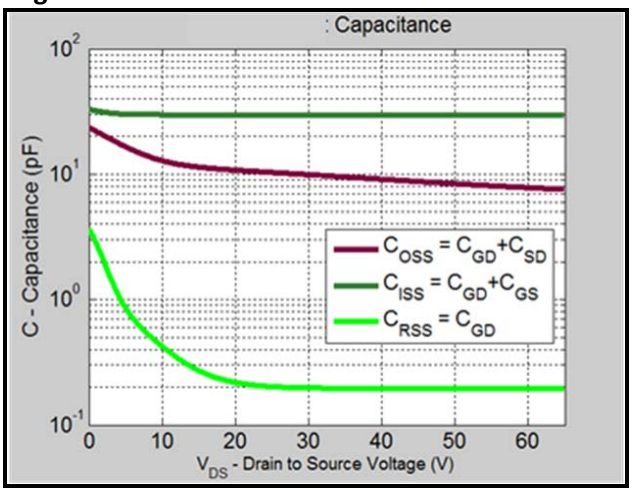


Figure 5a:



Linear Scale

Figure 5b:



Log Scale

Figure 6:

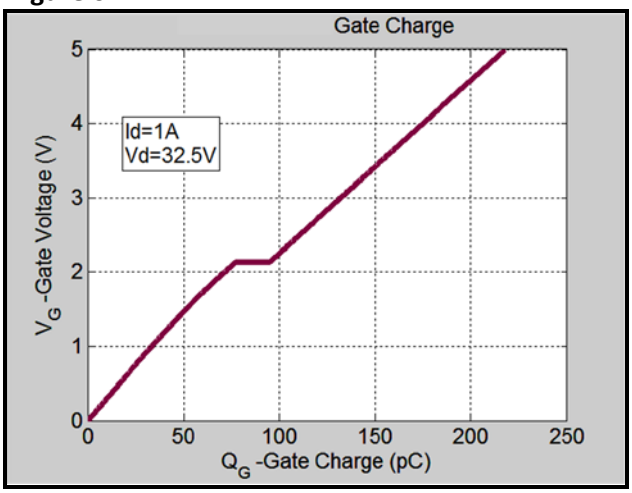


Figure 7:

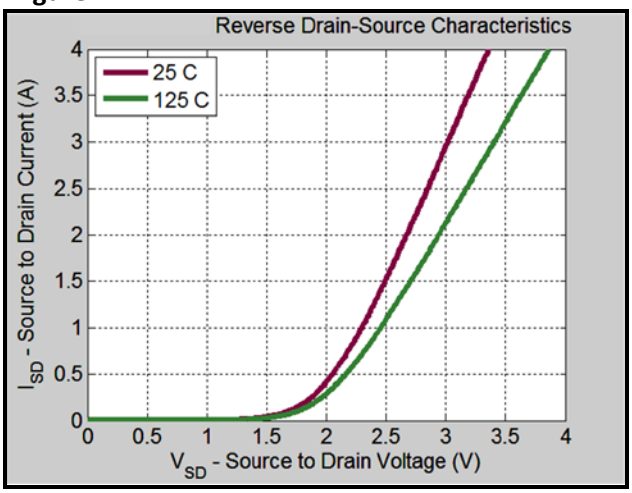


Figure 8:

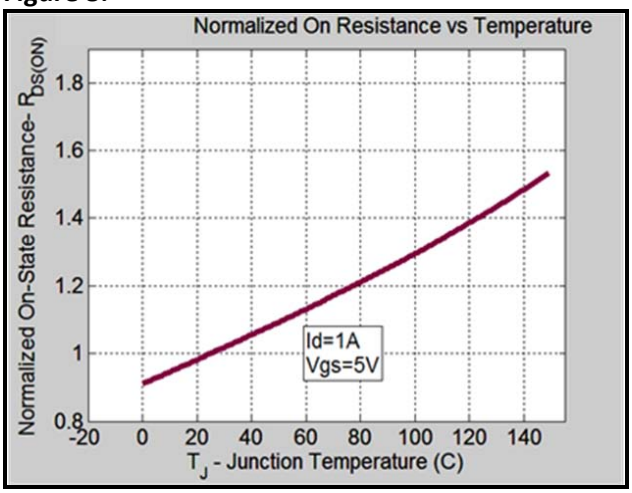
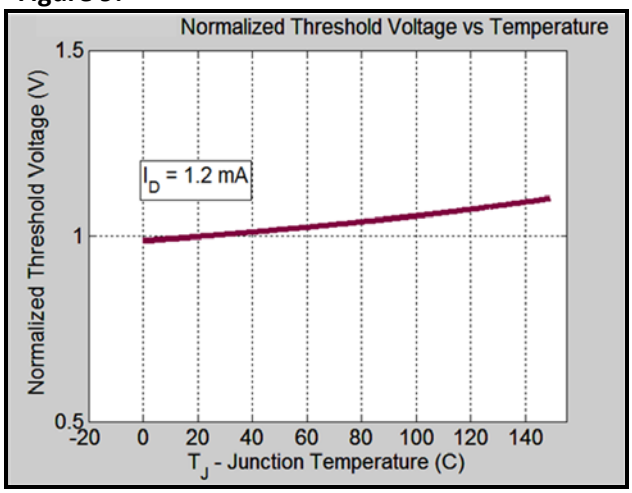


Figure 9:



All measurements were done with substrate shorted to source

S-PARAMETER CHARACTERISTICS

V_{GSQ} = 1.5 V, V_{DSQ} = 30 V, I_{DQ} = 0.25 A

Pulsed measurement, Heat-Sink Installed, Z_0 = 50 Ω

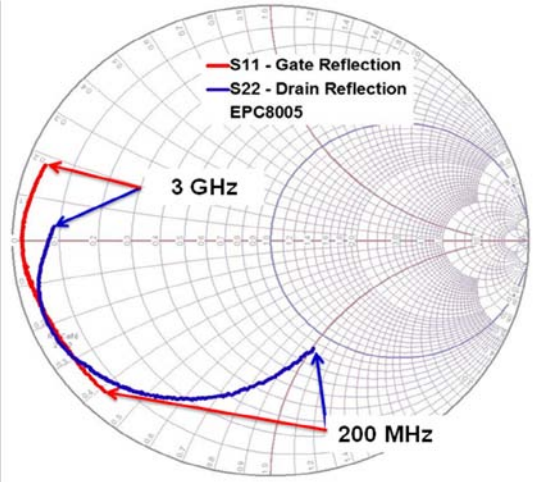


Figure 10: Smith Chart

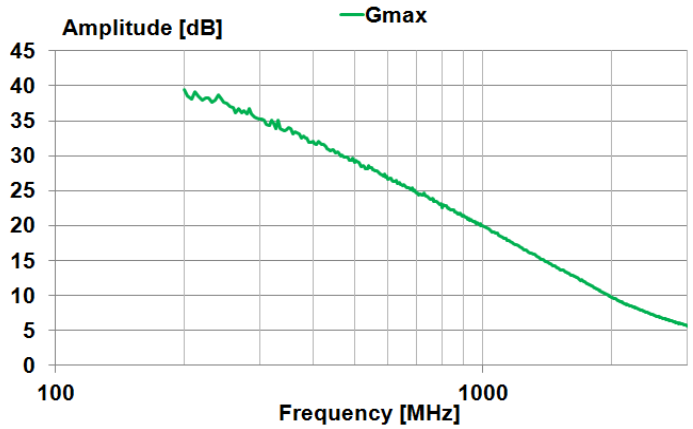


Figure 11: Gain Chart

Frequency [MHz]	Gate (Z_{GS}) [Ω]	Drain (Z_{DS}) [Ω]
200	2.92 – j20.49	42.43 – j50.08
500	1.86 – j8.15	10.61 – j31.19
1000	1.11 – j2.48	2.74 – j15.14
1200	0.95 – j1.07	1.96 – j11.73
1500	0.92 + j0.68	1.84 – j7.78
2000	1.02 + j3.11	2.53 – j3.42
2400	1.29 + j5.16	3.36 – j1.07
3000	1.80 + j9.03	4.29 + j1.95

Table 1: S-Parameter Table

Download S-parameter files at www.epc-co.com

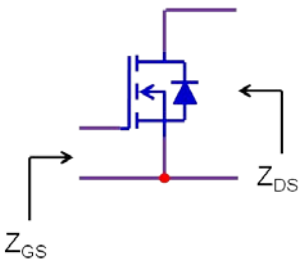


Figure 12: Device Reflection

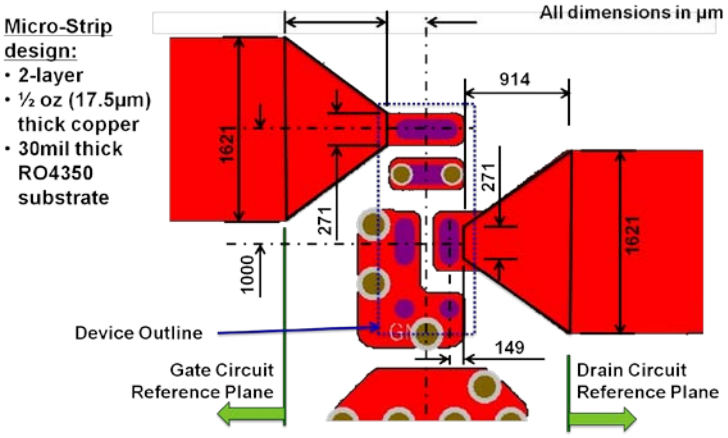
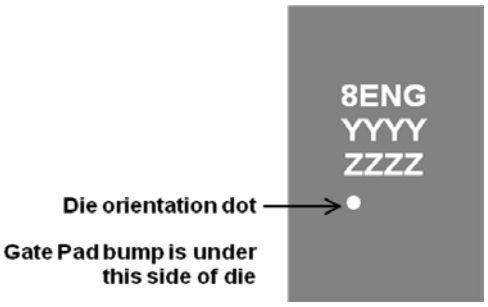


Figure 13: Taper and Reference Plane details – Device Connection

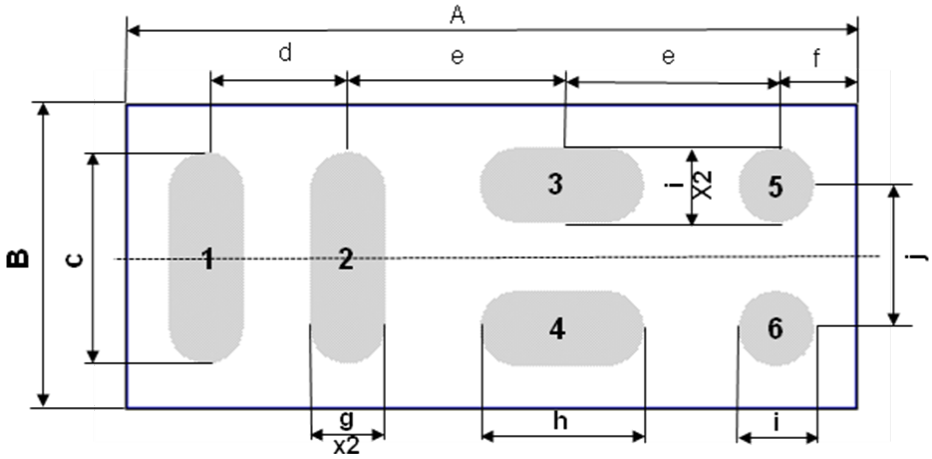
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC8005	8ENG	YYYY	ZZZZ

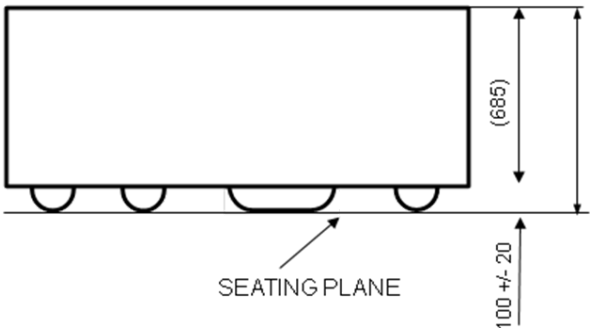
DIE OUTLINE

Solder Bar View



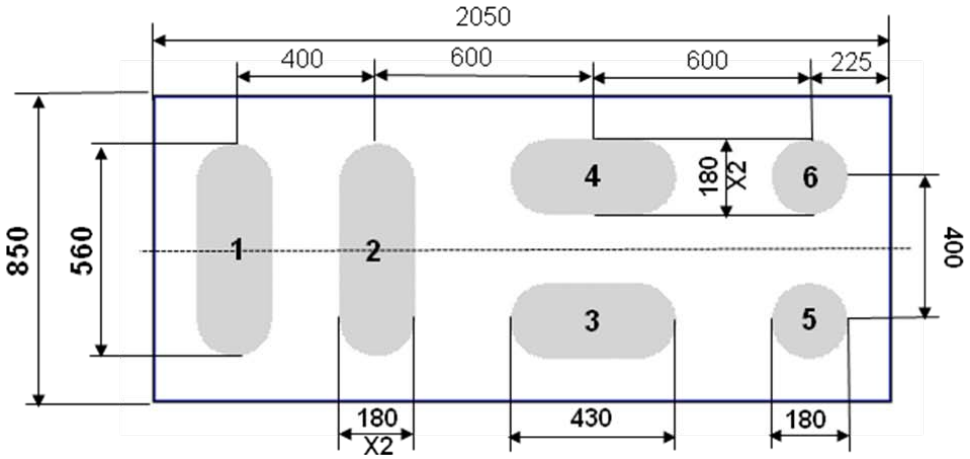
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2020	2050	2080
B	820	850	880
c	555	580	605
d	400	400	400
e	600	600	600
f	200	225	250
g	175	200	225
h	425	450	475
i	175	200	225
j	400	400	400

Side View



RECOMMENDED LAND PATTERN

(*units in µm)*



Pad no. 1 is Gate

Pad no. 2 is Source Return for Gate Driver

Pad no. 3 and 5 are Source

Pad no. 4 is Drain

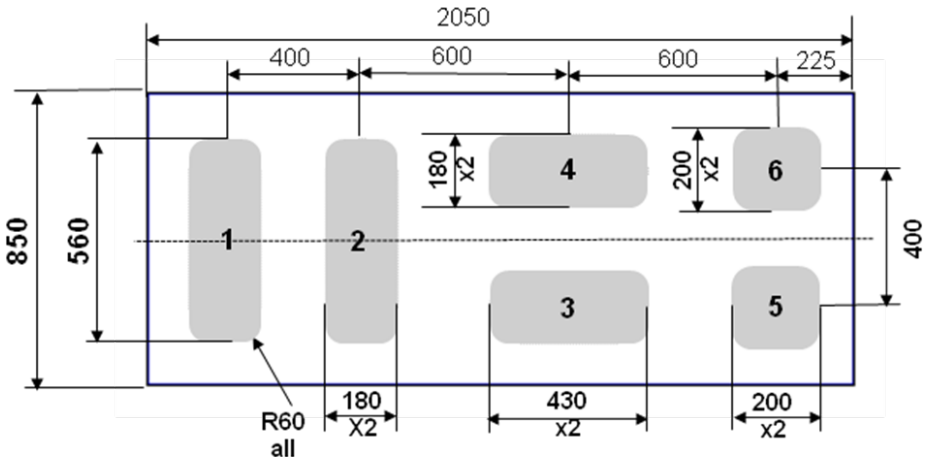
Pad no. 6 is Substrate

Land pattern is solder mask defined

Solder mask opening is 10 µm smaller per side than bump

RECOMMENDED STENCIL

(*units in µm)*



Pad no. 1 is Gate

Pad no. 2 is Source Return for Gate Driver

Pad no. 3 and 5 are Source

Pad no. 4 is Drain

Pad no. 6 is Substrate

Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.

Note that openings for pads 5 & 6 are larger than solder mask opening.

Revised September, 2013