



# STW75NF30

N-channel 300 V, 0.037  $\Omega$ , 60 A, TO-247  
low gate charge STripFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>w</sub>
STW75NF30	300 V	< 0.045 $\Omega$	60 A	320 W

- Exceptional dv/dt capability
- Low gate charge
- 100% Avalanche tested

## Application

- Switching applications

## Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters

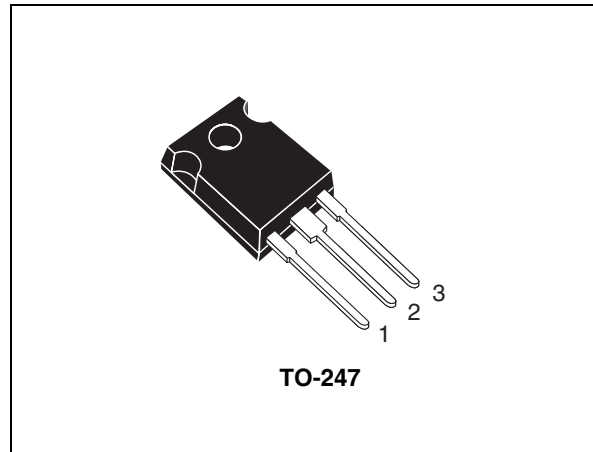


Figure 1. Internal schematic diagram

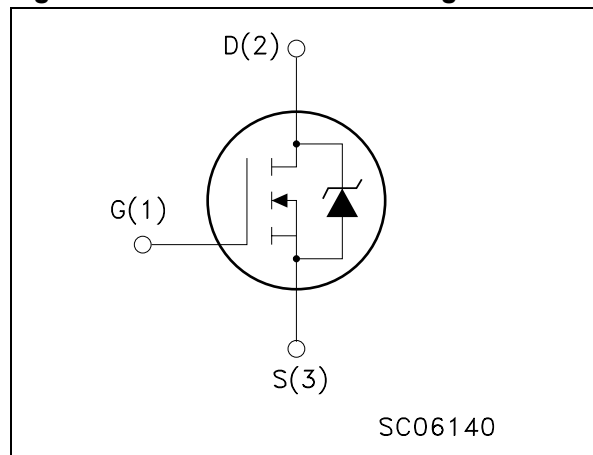


Table 1. Device summary

Order code	Marking	Package	Packaging
STW75NF30	75NF30	TO-247	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	300	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	60	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	37.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	240	A
	Derating factor	2.56	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	12	V/ns
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	320	W
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 60\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 80\% V_{(BR)DSS}$

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.39	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Max. value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	50	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	400	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	300			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{DS} = \pm 20 \text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$		0.037	0.045	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15 \text{ V}, I_D = 30 \text{ A}$		40		S
$C_{iss}$	Input capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0$		5930		pF
$C_{oss}$	Output capacitance			837		pF
$C_{rss}$	Reverse Transfer Capacitance			110		pF
$C_{oss \text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{DS} = 0 \text{ to } 240 \text{ V}, V_{GS} = 0$		462		pF
$R_G$	Intrinsic gate resistance	$f = 1 \text{ MHz open drain}$		1.55		$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 240 \text{ V}, I_D = 30 \text{ A},$ $V_{GS} = 10 \text{ V}$ <i>(see Figure 15)</i>		164		nC
$Q_{gs}$	Gate-source charge			36		nC
$Q_{gd}$	Gate-drain charge			69		nC

1. Pulsed: pulse duration = 300 $\mu s$ , duty cycle 1.5%

2.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 150\text{ V}$ , $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ , (see Figure 14)		115		ns
$t_r$	Rise time			87		ns
$t_{d(off)}$	Turn-off delay time			141		ns
$t_f$	Fall time			101		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				60	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				240	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 60\text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 60\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 19)		252		ns
$Q_{rr}$	Reverse recovery charge			2.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			20		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 60\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ $T_j = 150^\circ\text{C}$ (see Figure 19)		316		ns
$Q_{rr}$	Reverse recovery charge			3.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			23.2		A

1. Pulse with limited by maximum temperature
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

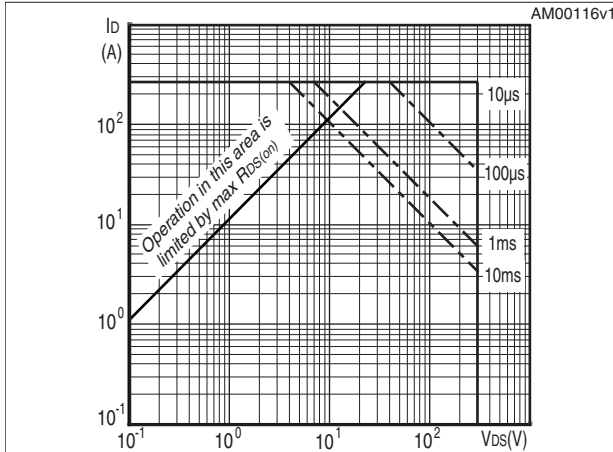


Figure 3. Thermal impedance

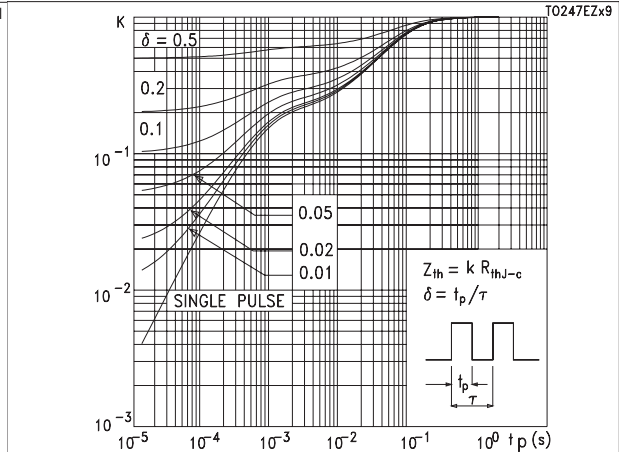


Figure 4. Output characteristics

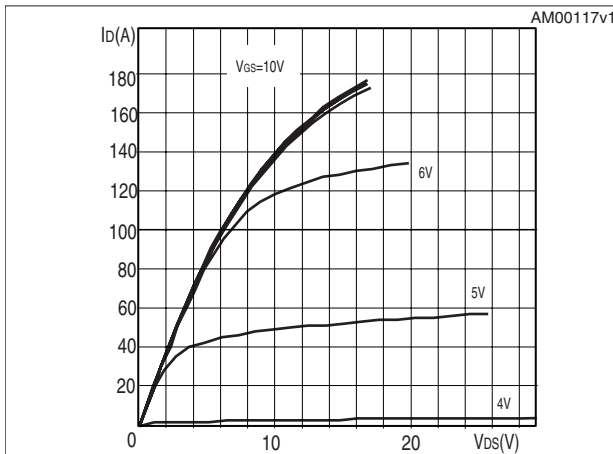


Figure 5. Transfer characteristics

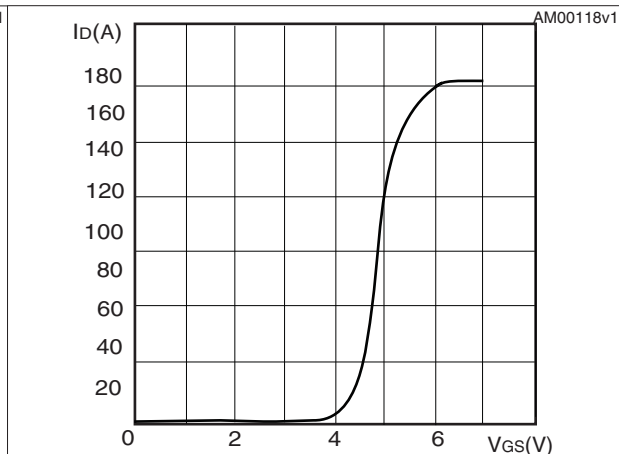


Figure 6. Normalized  $BV_{DSS}$  vs temperature

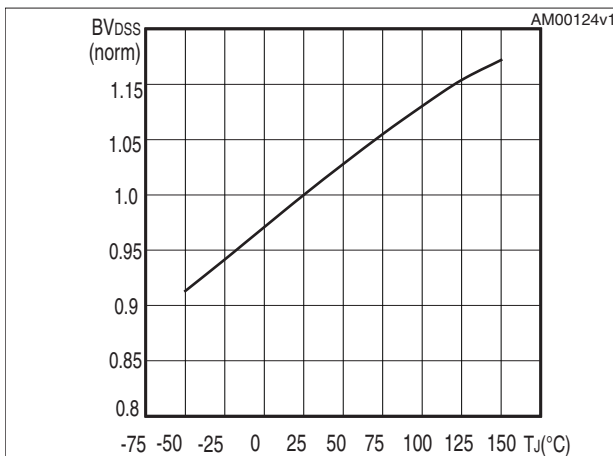


Figure 7. Static drain-source on resistance

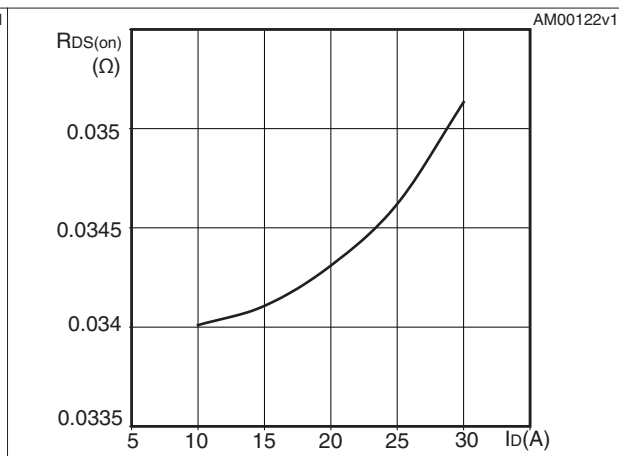


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

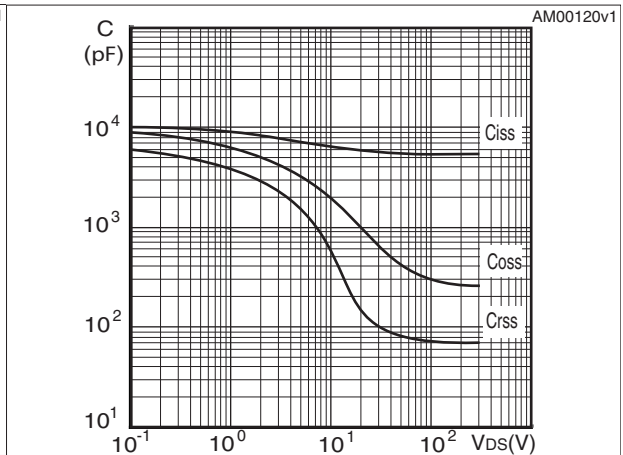
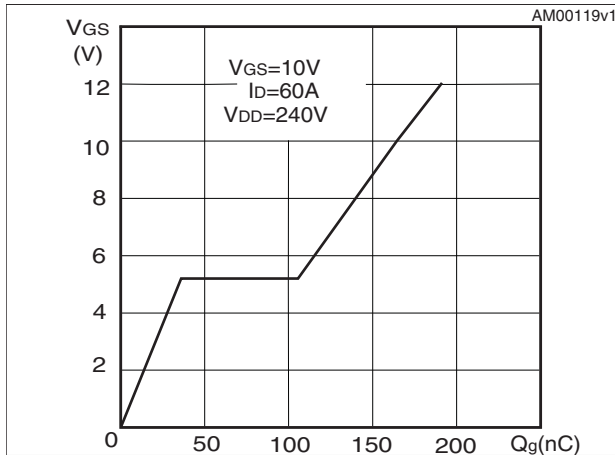


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on-resistance vs temperature

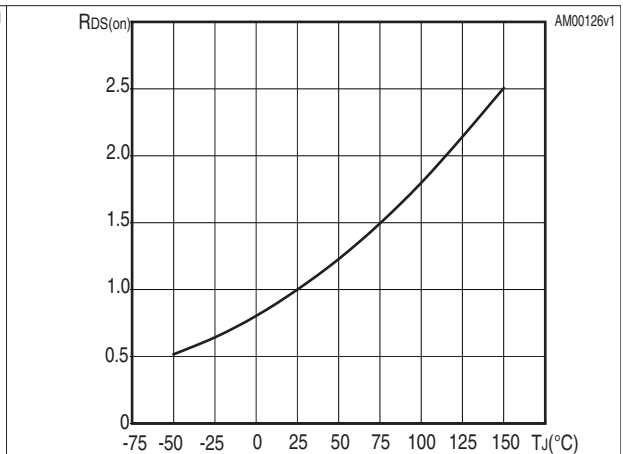
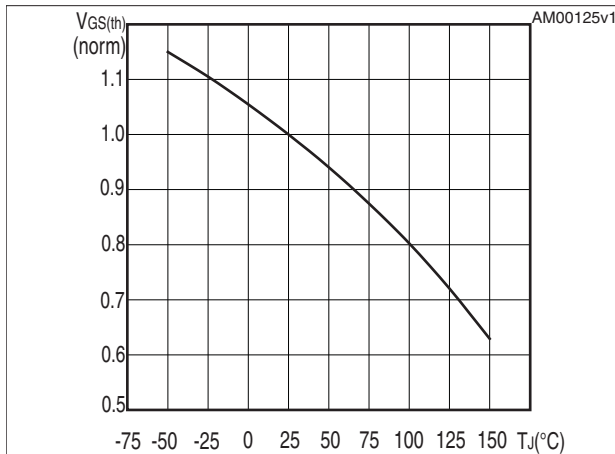
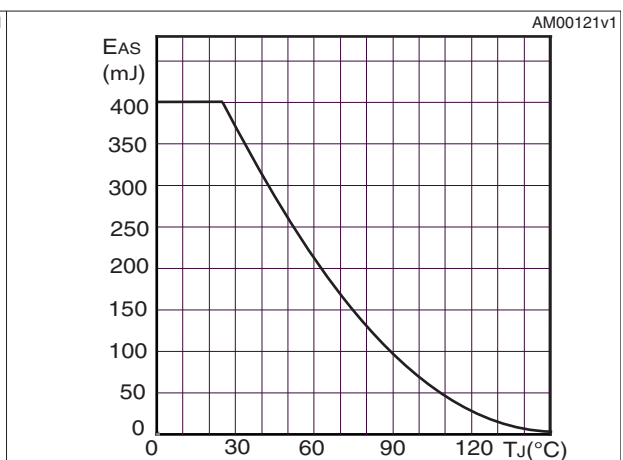
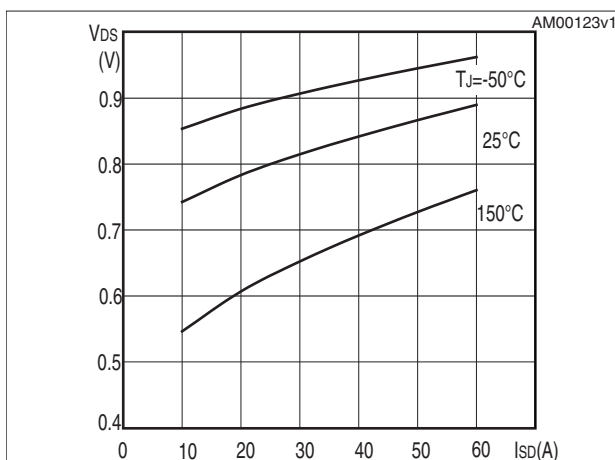


Figure 12. Source-drain diode forward characteristics

Figure 13. Maximum avalanche energy vs temperature



### 3 Test circuits

Figure 14. Switching times test circuit for resistive load

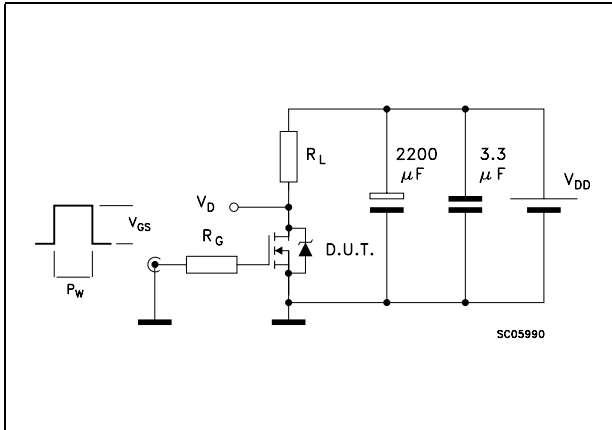


Figure 15. Gate charge test circuit

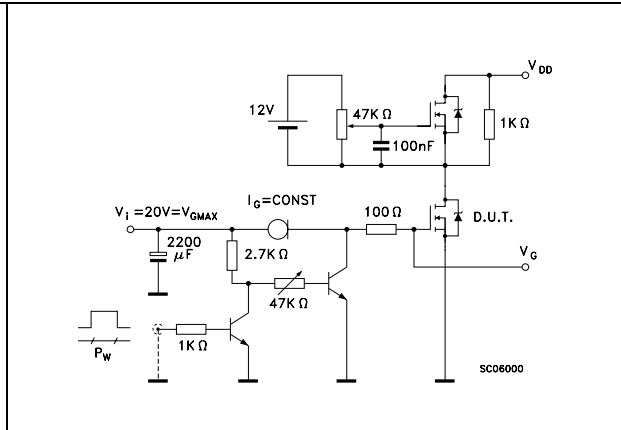


Figure 16. Test circuit for inductive load switching and diode recovery times

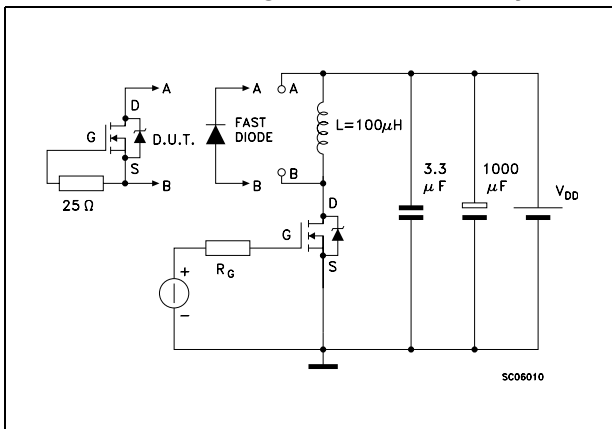


Figure 17. Unclamped inductive load test circuit

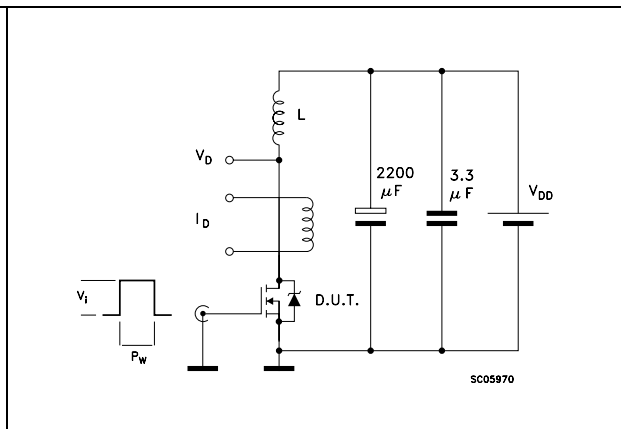


Figure 18. Unclamped inductive waveform

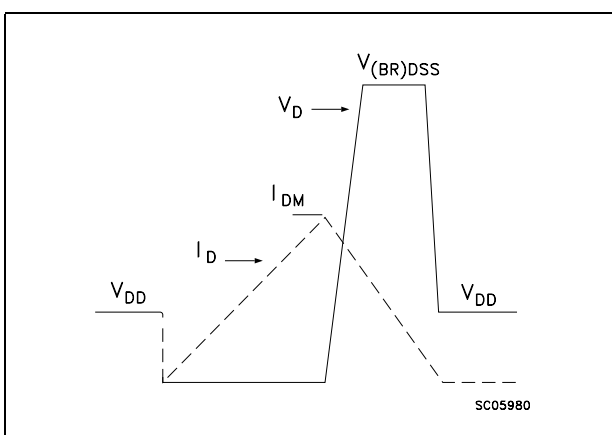
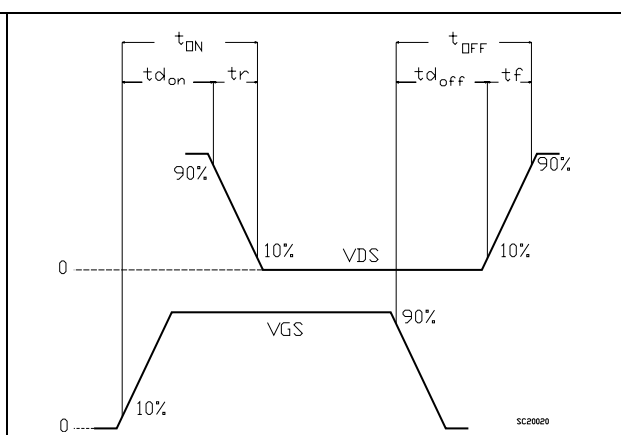


Figure 19. Switching time waveform



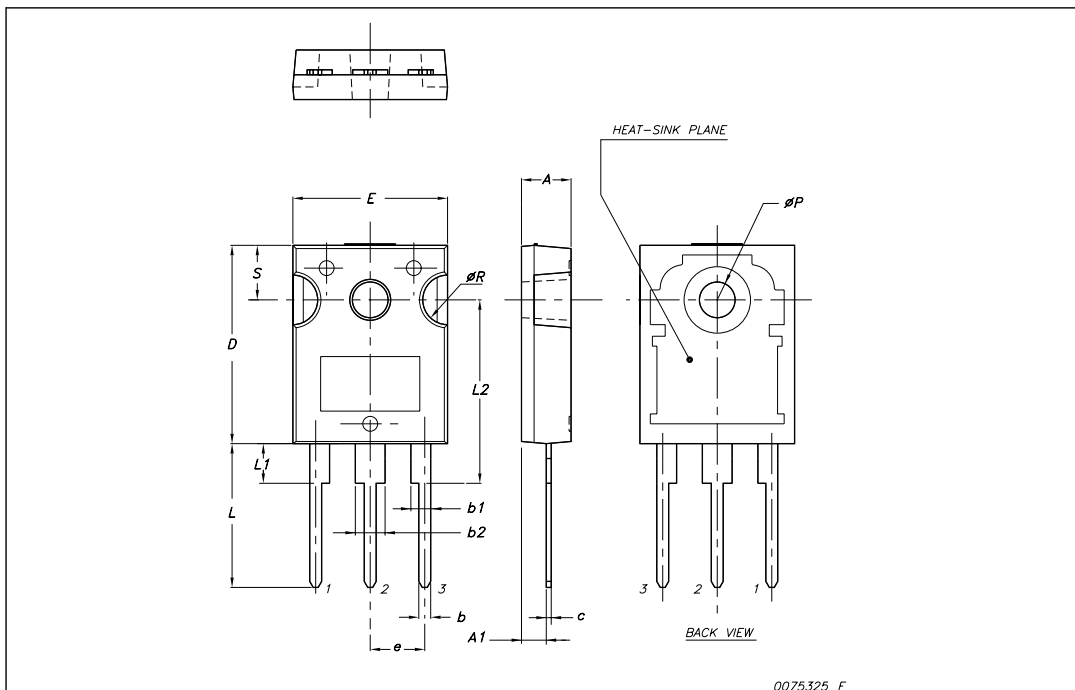


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**TO-247 Mechanical data**

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
23-Oct-2007	1	First release
27-May-2008	2	New value inserted in <a href="#">Table 5: Dynamic</a>
15-Jul-2008	3	Document status promoted from preliminary data to datasheet

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