Improved Quad CMOS Analog Switches

DESCRIPTION

The DG201B, DG202B analog switches are highly improved versions of the industry-standard DG201A, DG202. These devices are fabricated in Vishay Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG201B and DG202B can handle up to ± 22 V input signals, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply voltages in the off condition.

The DG201B is a normally closed switch and the DG202B is a normally open switch. (see Truth Table.)

FEATURES

- ± 22 V supply voltage rating
- TTL and CMOS compatible logic
- Low on-resistance - $R_{DS(on)}$: 45 Ω
- Low leakage - $I_{D(on)}$: 20 pA
- Single supply operation possible
- Extended temperature range
- Fast switching - t_{ON}: 120 ns
- Low glitching - Q: 1 pC

BENEFITS

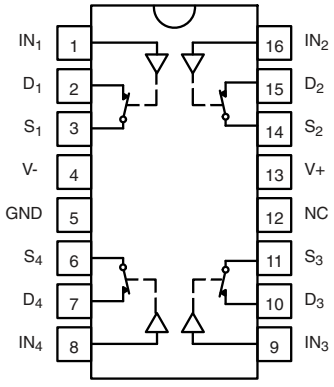
- Wide analog signal range
- Simple logic interface
- Higher accuracy
- Minimum transients
- Reduced power consumption
- Superior to DG201A, DG202

APPLICATIONS

- Industrial instrumentation
- Test equipment
- Communications systems
- Disk drives
- Computer peripherals
- Portable instruments
- Sample-and-hold circuits
- Hi-Rel systems

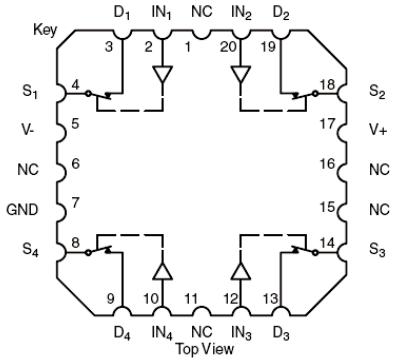
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG201B/DG202B
Dual-In-Line, CerDIP



Top View

DG201B/DG202B
LCC



Top View

TRUTH TABLE		
Logic	DG201B	DG202B
0	On	Off
1	Off	On

Notes

- Logic "0" ≤ 0.8 V
- Logic "1" ≥ 2.4 V

ORDERING INFORMATION (Hi-Rel)						
PART	CONFIGURATION	TEMP. RANGE	PACKAGE	ORDERING PART	GENERIC	DSCC NUMBER
DG201B	SPST x 4, NC	- 55 °C to 125 °C	16-pin CerDIP	DG201BAK	DG201BAK	-
				DG201BAK-E3	DG201BAK-E3	-
				DG201BAK/883	DG201BAK/883	5962-8671604MEA (Vishay qualified, DSCC approval in progress)
			LCC-20	DG201BAZ/883	DG201BAZ/883	5962-8671604M2A (Vishay qualified, DSCC approval in progress)
DG202B	SPST x 4, NO	- 55 °C to 125 °C	16-pin CerDIP	DG202BAK	DG202BAK	-
				DG202BAK-E3	DG202BAK-E3	-
				DG202BAK/883	DG202BAK/883	5962-8671605MEA (Vishay qualified, DSCC approval in progress)
			LCC-20	DG202BAZ/883	DG202BAZ/883	5962-8671605M2A (Vishay qualified, DSCC approval in progress)

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Voltages Referenced to V-		44	V
GND		25	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current (any terminal)		30	mA
Peak Current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(A suffix)	- 65 to 150	°C
Power Dissipation (Package)[b]	16-pin CerDIP[c]	900	mW
	LCC-20[d]	750	

Notes
a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 12 mW/°C above 75 °C.
d. Derate 10 mW/°C above 75 °C.

SCHEMATIC DIAGRAM (typical channel)

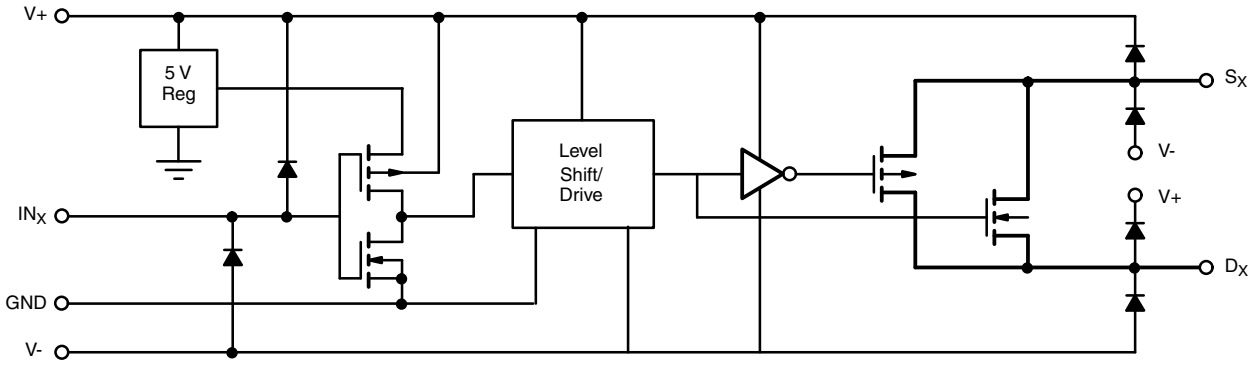


Fig. 1

SPECIFICATIONS[a]							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = - 15 V V_{IN} = 2.4 V, 0.8 V[f]	TEMP.[b]	TYP.[c]	A SUFFIX - 55 °C to 125 °C MIN.[d]	 MAX.[d]	UNIT
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	-	- 15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = ± 10 V, I_S = 1 mA	Room	45	-	85	Ω
			Full	-	-	100	
$R_{DS(on)}$ Match	$\Delta R_{DS(on)}$		Room	2	-	-	
Source Off Leakage Current	$I_{S(off)}$	V_S = ± 14 V, V_D = ± 14 V	Room	± 0.01	- 0.5	0.5	nA
			Full	-	- 20	20	
Drain Off Leakage Current	$I_{D(off)}$	V_S = ± 14 V, V_D = ± 14 V	Room	± 0.01	- 0.5	0.5	
			Full	-	- 20	20	
Drain On Leakage Current	$I_{D(on)}$	V_S = ± 14 V, V_D = ± 14 V	Room	± 0.02	- 0.5	0.5	
			Full	-	- 40	40	
Digital Control							
High Input Voltage	V_{INH}		Full	-	2.4	-	V
Low Input Voltage	V_{INL}		Full	-	-	0.8	
Input Current	I_{INH} or I_{INL}	V_{INH} or V_{INL}	Full	-	- 1	1	µA
Input Capacitance	C_{in}		Room	5	-	-	pF
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = 2 V see switching time test circuit	Room	120	-	300	ns
			Full	-	-	-	
Turn-Off Time	t_{Off}		Room	65	-	200	
			Full	-	-	-	
Charge Injection	Q	C_L = 1000 pF, V_g = 0 V, R_g = 0 Ω	Room	1	-	-	pC
Source Off Capacitance	$C_{S(off)}$	V_S = 0 V, f = 1 MHz	Room	5	-	-	pF
Drain Off Capacitance	$C_{D(off)}$		Room	5	-	-	
Channel On Capacitance	$C_{D(on)}$	V_D = V_S = 0 V, f = 1 MHz	Room	16	-	-	
Off Isolation	OIRR	C_L = 15 pF, R_L = 50 Ω, V_S = 1 V_{RMS}, f = 100 kHz	Room	90	-	-	dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	95	-	-	
Power Supply							
Positive Supply Current	I+	V_{IN} = 0 V or 5 V	Room	-	-	50	µA
			Full	-	-	100	
Negative Supply Current	I-		Room	-	- 1	-	
			Full	-	- 5	-	
Power Supply Range for Continuous Operation	V_{OP}		Full	-	± 4.5	± 22	V

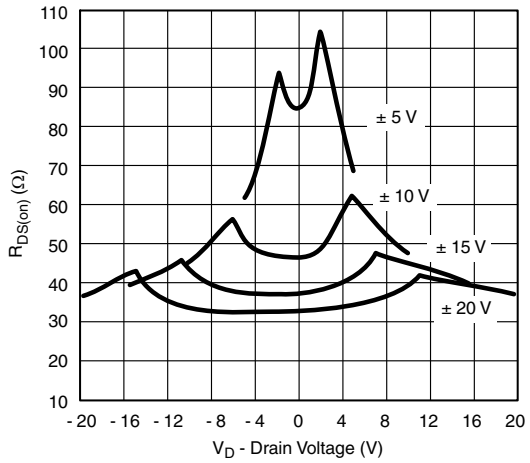
SPECIFICATIONS[a] (Single Supply)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 12 V, V- = 0 V V_{IN} = 2.4 V, 0.8 V[f]	**TEMP.**[b]	**TYP.**[c]	**A SUFFIX - 55 °C to 125 °C** **MIN.**[d]	**MAX.**[d]	**UNIT**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	-	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = 3 V, 8 V, I_S = 1 mA	Room	90	-	160	Ω
			Full	-	-	200	
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = 8 V see switching time test circuit	Room	120	-	300	ns
Turn-Off Time	t_{OFF}		Room	60	-	200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room	4	-	-	pC
Power Supply							
Positive Supply Current	I+	V_{IN} = 0 V or 5 V	Room	-	-	50	µA
			Full	-	-	100	
Negative Supply Current	I-		Room	-	- 1	-	
			Full	-	- 5	-	
Power Supply Range for Continuous Operation	V_{OP}		Full	-	4.5	25	V

Notes

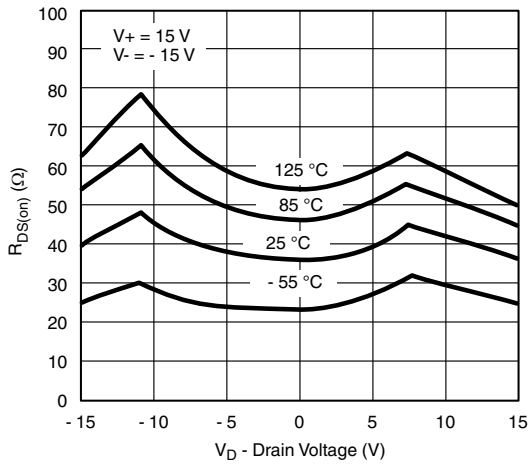
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

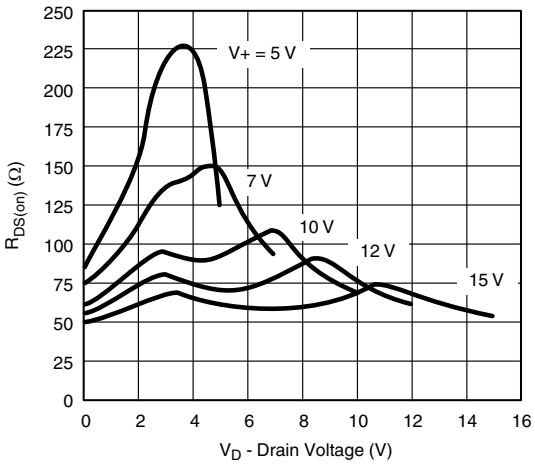
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



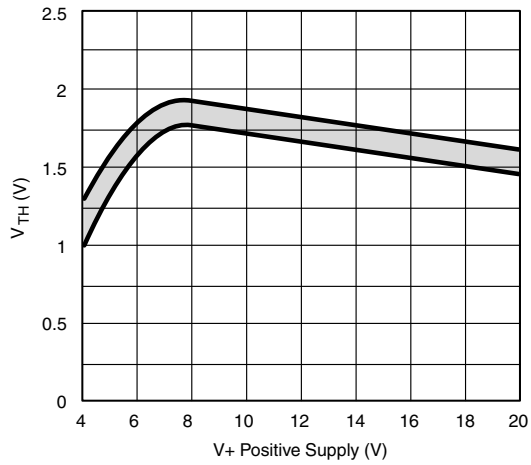
$R_{DS(on)}$ vs. V_D and Power Supply Voltages



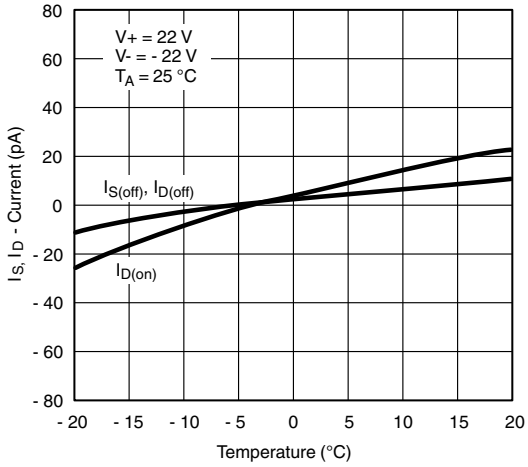
$R_{DS(on)}$ vs. V_D and Temperature



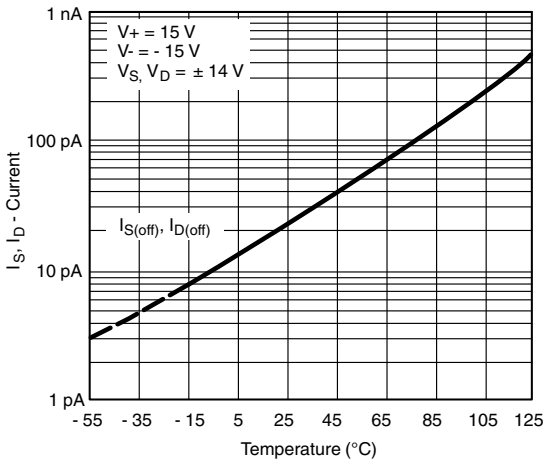
$R_{DS(on)}$ vs. V_D and Single Power Supply Voltages



Input Switching Threshold vs. Supply Voltage

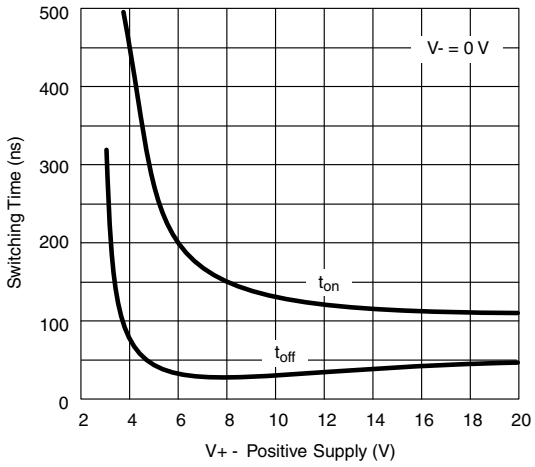


Leakage Currents vs. Analog Voltage

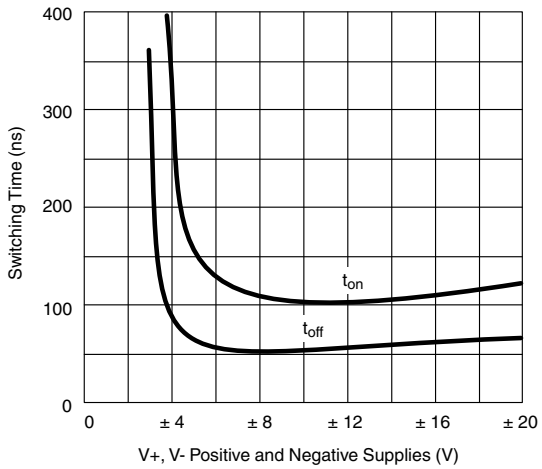


Leakage Currents vs. Temperature

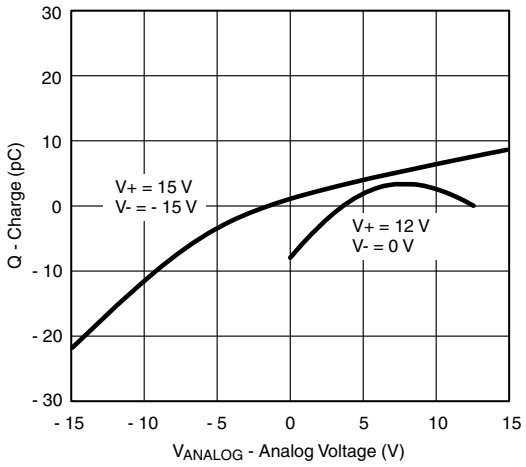
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



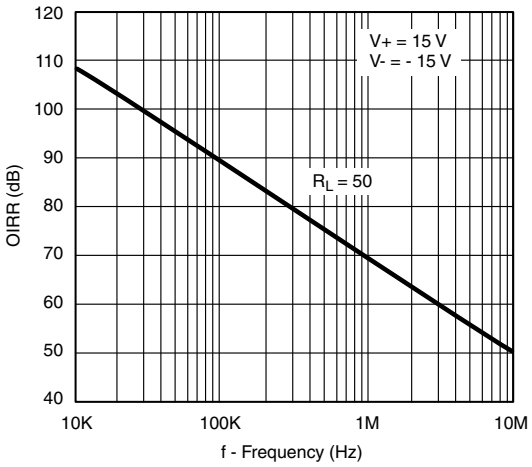
Switching Time vs. Single Supply Voltage



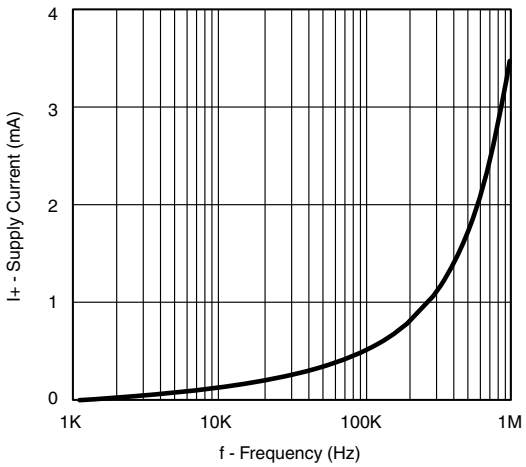
Switching Time vs. Power Supply Voltage



Q_S, Q_D - Charge Injection vs. Analog Voltage

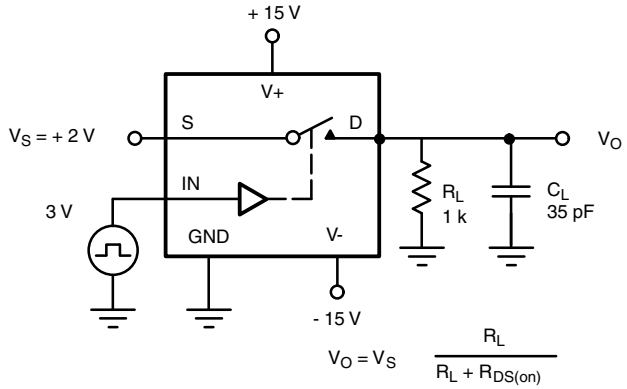


Off Isolation vs. Frequency



Supply Current vs. Switching Frequency

TEST CIRCUITS



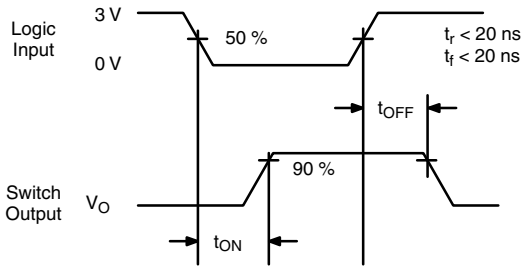


Fig. 2 - Switching Time

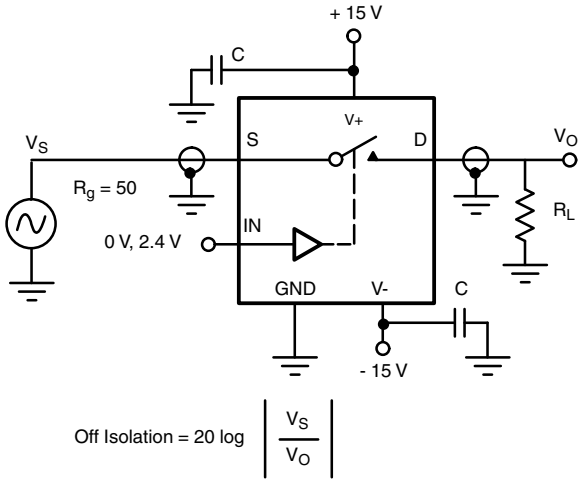


Fig. 3 - Off Isolation

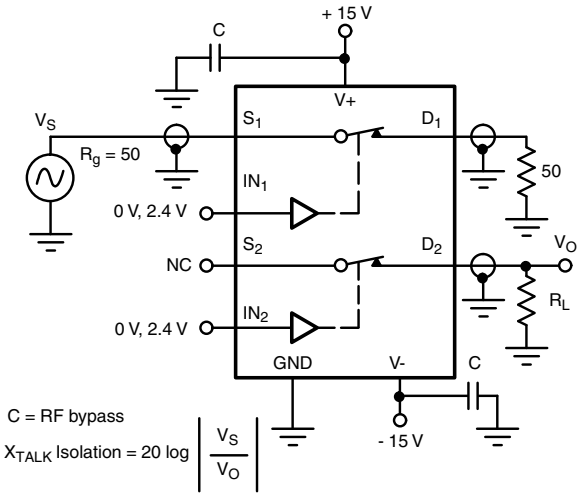
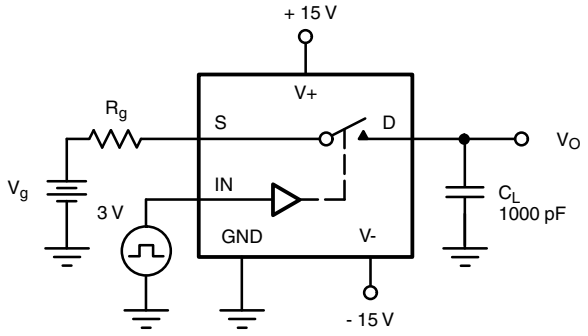
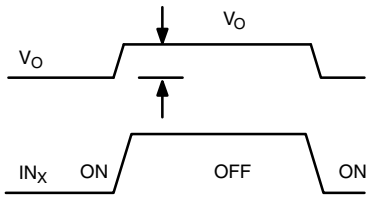


Fig. 4 - Channel-to-Channel Crosstalk





V_O = measured voltage error due to charge injection
The charge injection in coulombs is Q = C_L x V_O

Fig. 5 - Charge Injection

APPLICATIONS

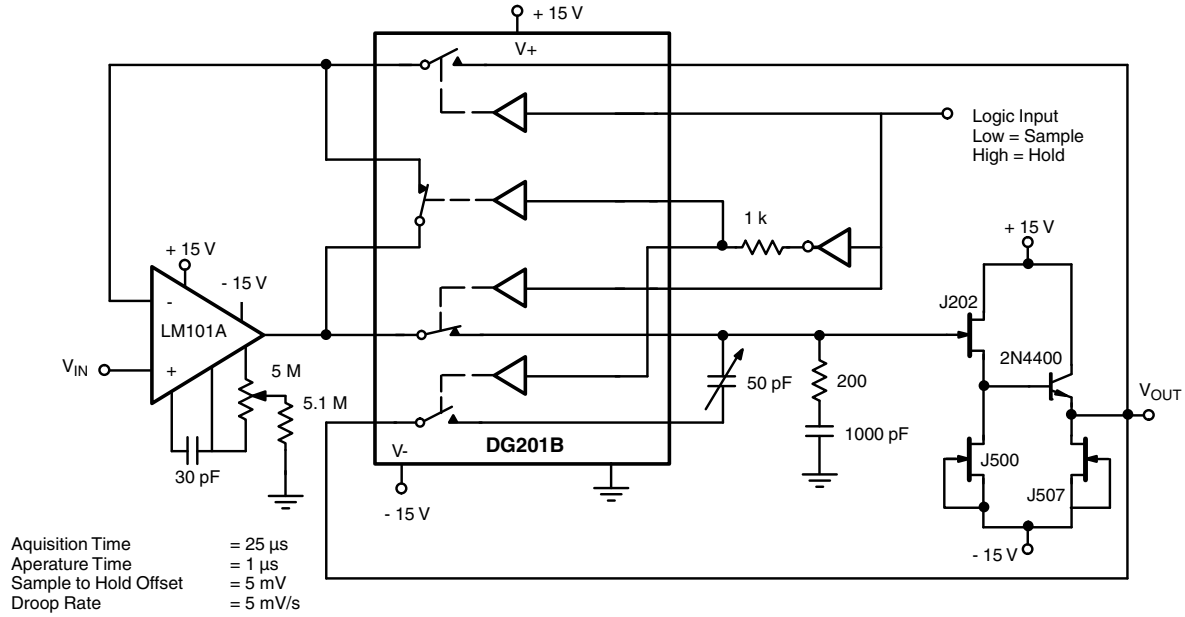


Fig. 6 - Sample-and-Hold

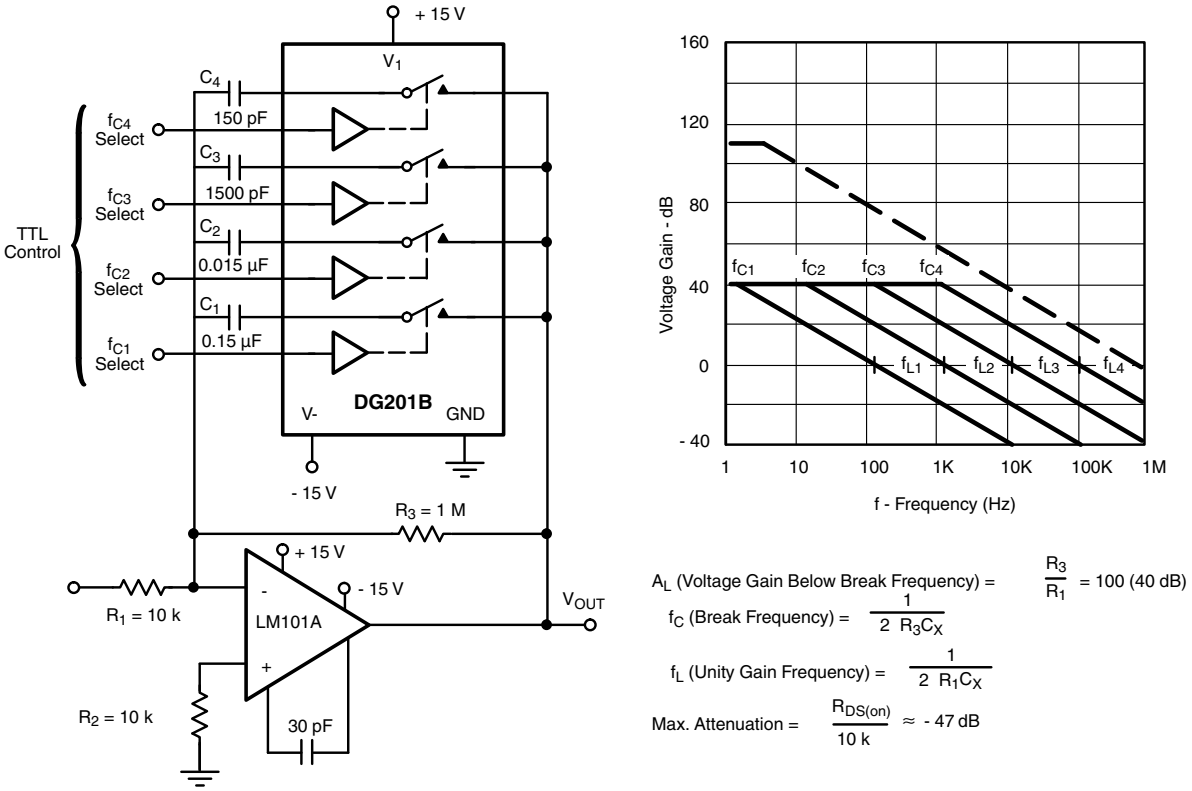


Fig. 7 - Active Low Pass Filter with Digitally Selected Break Frequency

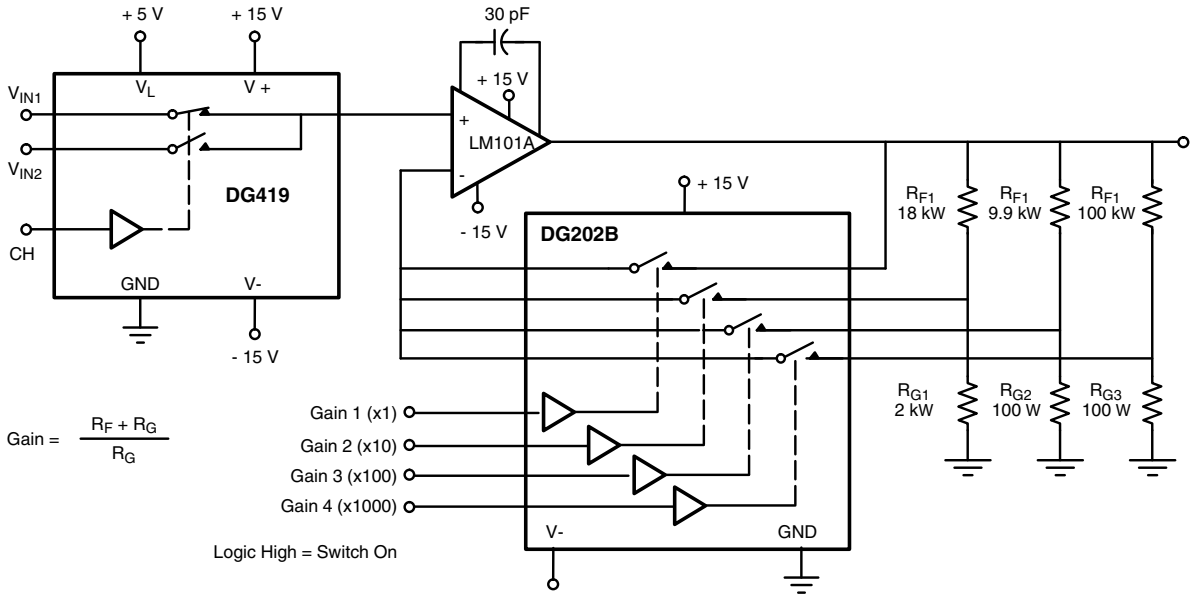
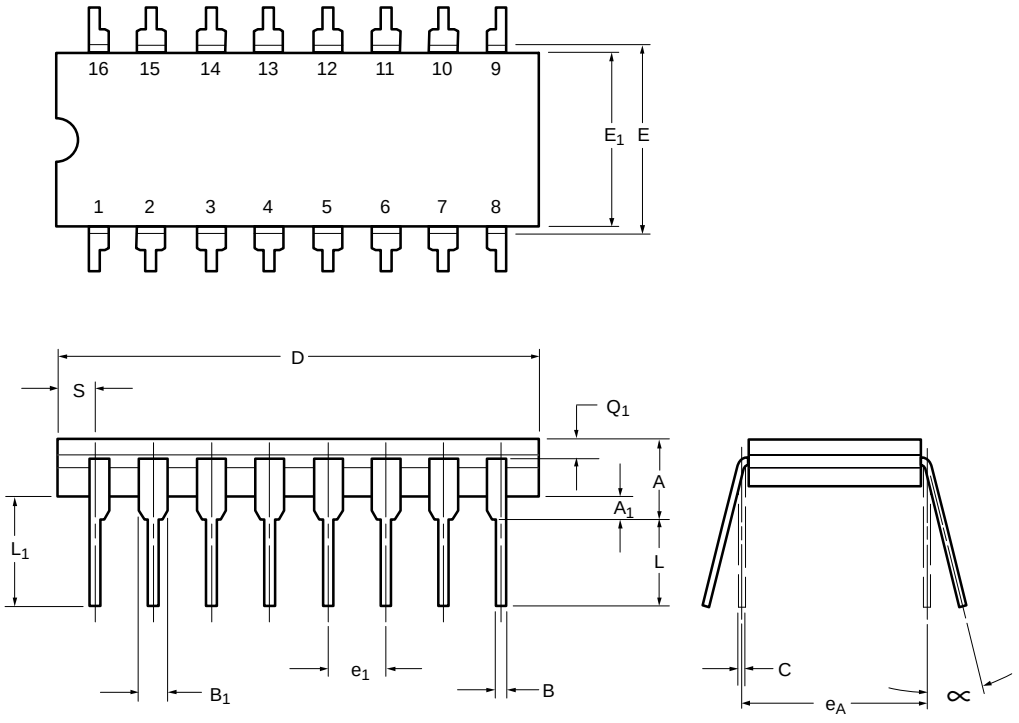


Fig. 8 -A Precision Amplifier with Digitally Programable Input and Gains

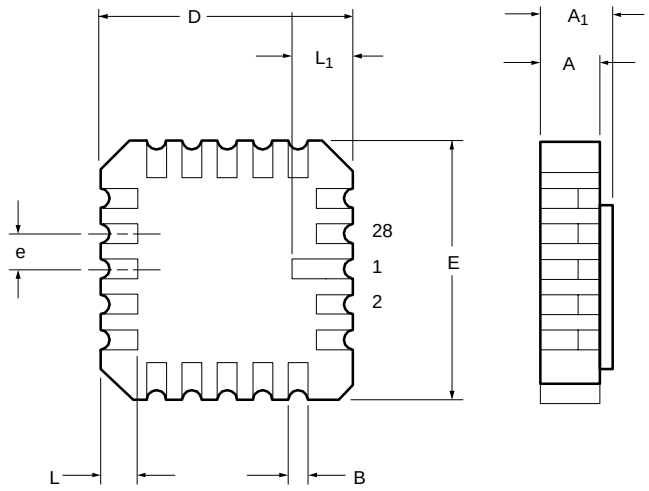
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63374.

CERDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B_1	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E_1	6.60	7.62	0.260	0.300
e_1	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L_1	3.81	5.08	0.150	0.200
Q_1	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
∝	0°	15°	0°	15°
ECN: S-03946—Rev. G, 09-Jul-01 DWG: 5403				

20-LEAD LCC



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A_1	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D	8.69	9.09	0.342	0.358
E	8.69	9.09	0.442	0.358
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L_1	1.96	2.36	0.077	0.093

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5321

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