Product Brief

MC92603PB/D
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MC92603 Quad and MC92604 Dual Gigabit Ethernet Transceivers

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Overview

This document explains the basic fundamental features and functional operation of the MC92603 Quad and MC92604 Dual Gigabit Ethernet transceivers (GEt). The MC92603 is a quad device and each channel may be operated independently or in a 'trunking', word aligned, mode. The MC92604 is a two channel version and is offered in a smaller package. Although the remainder of this document discusses the MC92603, the attributes are the same for the MC92604.

The Gigabit Ethernet transceiver was designed with the intent to meet the requirements of **IEEE Std 802.3-2002®**. It was designed to fully support full-duplex GMII or TBI PHY applications including the reduced RGMII or RTBI de facto interfaces. Each channel also has its own independent MDIO register set as specified in the above standard

The MC92603 GEt is designed as two parts in one. It may be configured as either a 1 gigabit backplane SERDES functionally similar to the MC92600, 1.25 Gbaud Quad SERDES, or as a quad 1 gigabit Ethernet GMII or TBI PHY.

The GEt is a high-speed, full-duplex, serial data interface device that can be used to transmit data between chips across a board, through a backplane, or through cabling, as well as to interface to GBIC/SFP modules. The multi-channel devices have transceivers that transmit and receive coded data at a rate of 1.0 Gbps through each 1.25 gigabaud link.

The MC92603 is built upon the proven transceiver technology of the MC92600 and MC92602 devices. Carefully designed for low power consumption, its 0.25 micron CMOS implementation nominally consumes less than 1 W with all links operating at full speed when in the backplane interface mode.

The MC92603 features transmit FIFOs and source synchronous transmit clocks per channel to further simplify interfacing. And finally, **IEEE Std 1149.1** JTAG boundary scan is added for board test support.

Features

The MC92603 and MC92604 have two applications oriented operating modes depending upon configuration. It may be used as a backplane SERDES or as an Ethernet PHY.

Common Features

- Full-duplex differential data links.
- Selectable speed range: 1.25 Gbaud or 0.625 Gbaud.
- Low power, approximately less than 1W under typical conditions, while operating in backplane mode with all transceivers at full speed.
- Internal 8B/10B encoder/decoder that may be bypassed.
- Source synchronous parallel data input interfaces.
- Selectable: Source aligned or source centered timing on the receiver output interfaces.
- DDR (RGMII/RTBI), source synchronous, 4-/5-bit optional interfaces.
- Parallel interfaces may be either LVTTL or SSTL_2.
- Transmit data clock is selectable between per-channel transmit clock or channel 'A' transmit clock.
- Received data may be clocked to the recovered clock or to the reference clock frequencies.
- Unused transceiver channels may be individually disabled.
- Drives 50-Ω or 75-Ω media (100-Ω or 150-Ω differential) for lengths of up to 1.5 meters board/backplane, or 10 meters of coax.
- Tolerates a frequency offset between the transmitter and receiver of ±250ppm.
- Link inputs have on-chip receiver termination and are "hot swap" compatible.
- Differential LVPECL reference clock input with single-ended LVCMOS input option.
- Two single-ended buffered reference clock outputs to be used as clock source for associated MAC interface logic.
- Built-in, at speed, self test for production testing and on-board diagnostics.
- **IEEE Std 1149.1** JTAG boundary scan test support.

Backplane Application Features

- Link-to-link synchronization supports aligned, multi-channel, word transfers. Synchronization mechanism tolerates up to 40 bit-times of link-to-link media delay skew.
- Supports three options for word synchronization including disparity based word sync events for compatibility with legacy transceivers.
- Selectable COMMA code group alignment mode enables aligned or unaligned transfers.

Ethernet Friendly Features

- Provides the PCS and PMA layers for Ethernet PHYs as specified in **IEEE Std 802.3-2000**.
- MDIO slave interface and registers as defined in **IEEE Std 802.3-2000** is fully supported.
- Supports rate adaption within IPG for Jumbo frames up to 16K bytes.

General Parameters

The MC92603 and MC92604 are designed in a 0.25µ lithography, HiP4 CMOS, 5 layer metal process.

The core logic and high speed serial link I/O require a 1.8 Volt power source while the parallel data interfaces may be 3.3 V LVTTL or 2.5 V SSTL.

The MC92603 is packaged in a 256 pin MAP Ball Grid Array which has a body size of 17 mm square. The package for the MC92604 is TBD.

Block Diagram

The MC92603 is a highly integrated device containing all of the logic needed to facilitate the application and test of a high-speed serial interface. No external components, other than the normal power supply decoupling network are required. A block diagram of the MC92603 GEt device is shown in Figure 1.

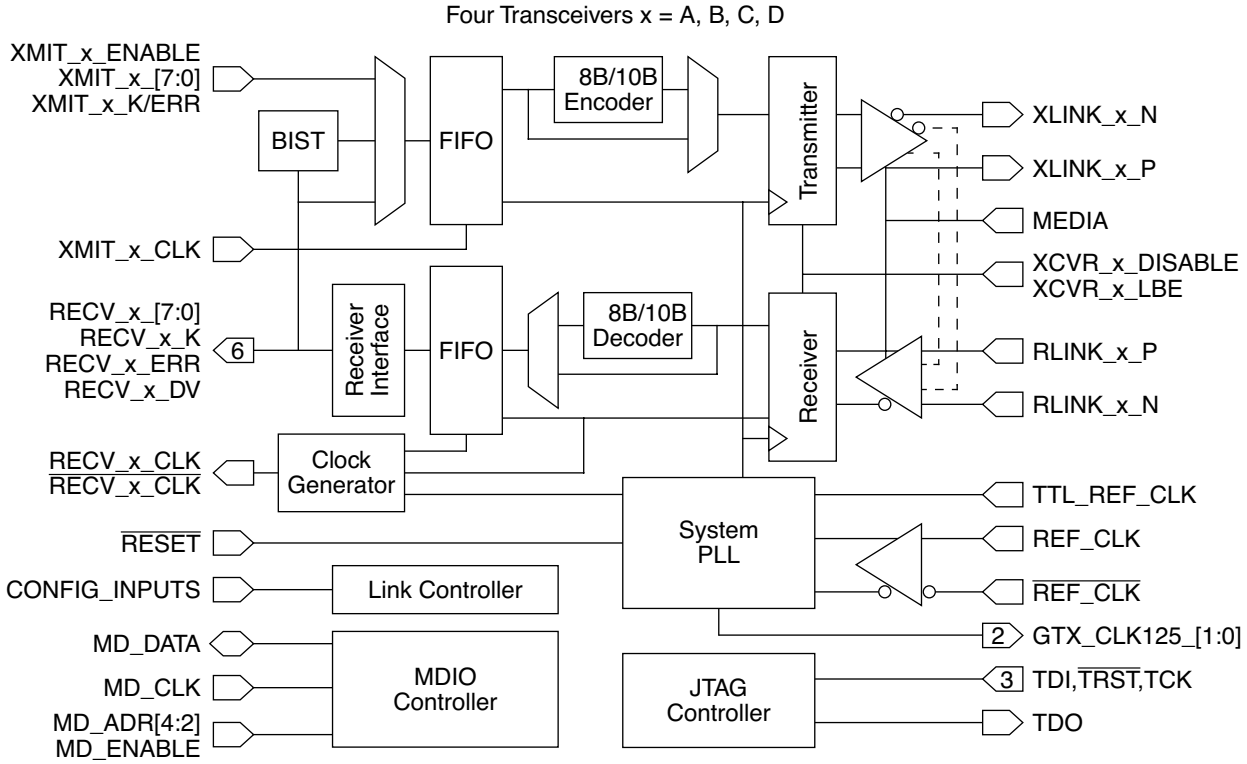

Figure 1. MC9603 Block Diagram

The MC92603 and MC92604 perform the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer for 1000BASE-X PHY as defined in clause 36 of the **IEEE 802.3-2002** specification.

Figure 2 shows a typical application for the MC92603. It may be used as a Quad 1000BASE-X PHY or is backplane applications. On high density line cards with a large number of Gig Ethernet ports it is desirable to use the RGMII interfaces to reduce the number of signal traces on the PCB.

The MC92603 and MC92604 may be used to interface directly to the gigabit MACs integrated into the MPC PowerQUICC III communications processors. They are also interface compatible to the C-Port, C-3, and C-5 network processors available from Motorola.

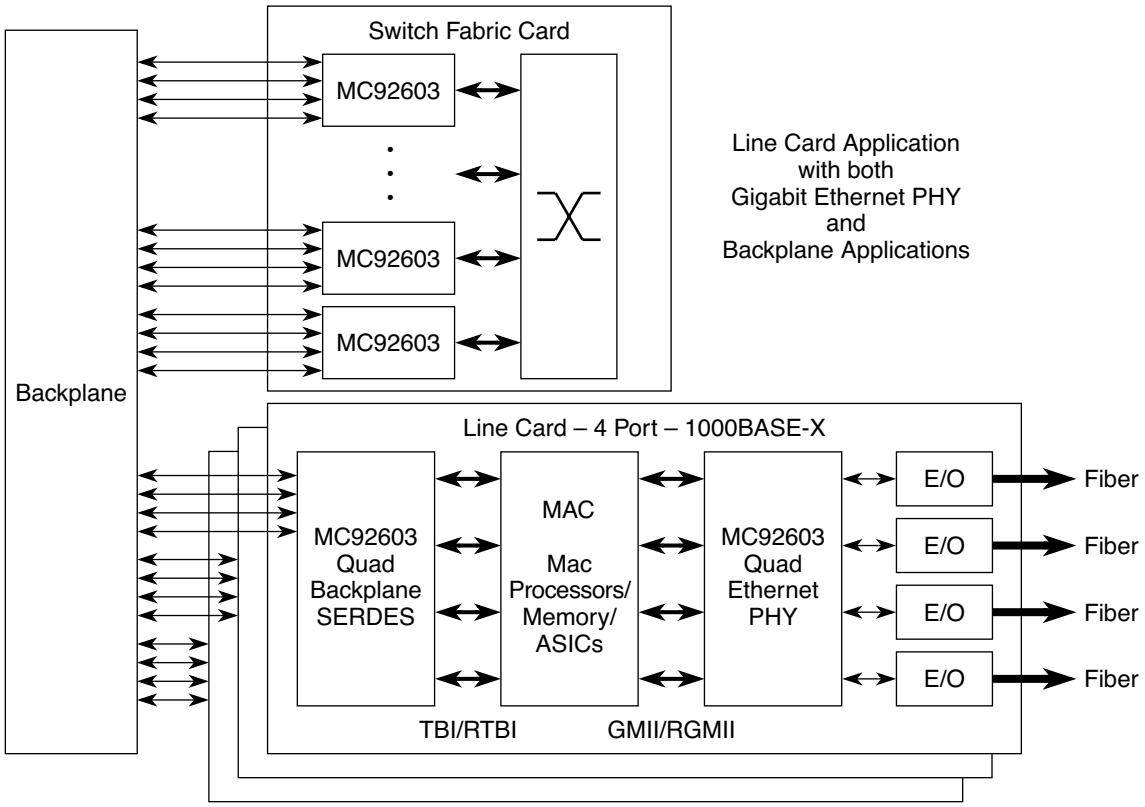

Figure 2. Phy and Backplane Application

Functional Summary

The transceivers send/receive differential data in one of two operating ranges. They may be operated in the high range with a maximum data rate of 1 Gbps (1.25 gigabaud) or at a half-rate of 500 Mbps (625 megabaud). The data transfer rate is determined by the state of the half speed enable (HSE) input and the frequency of the reference clock. Any frequency and resulting data rate with in the ranges shown in Table 1 may be used.

The reference clock inputs are differential LVPECL. Optionally, a single ended 3.3 Volt (LVCMOS/LVTTL) input clock source may be used.

Table 1. Legal Reference Clock Frequency Ranges

HSE	Reference Frequency Min. (MHz)	Reference Frequency Max (MHz)	Link Transfer Rate (Gigabaud)
Low	95.00	135.0	0.95 - 1.35
High	47.50	67.50	0.475 - 0.675

Transmitter Functionality

The MC92603 and MC92604 are versatile devices that may be used in backplane or Ethernet PHY applications. They may be configured in multiple data interface and operational modes. The following sections provide a basic functional description of the transmitter, its operational modes and data interfaces. Each transmitter takes data presented at its source synchronous parallel data input port, creates a transmission code group or character (if not pre-encoded), and serially transmits the code group out of the differential link output pads.

The transmitter driver is a controlled impedance driver. The impedance of the driver is programmable to 50- or 75-Ω through the MEDIA configuration signal. Drive impedance is 50-Ω when MEDIA is low and 75-Ω when high.

Interface Configuration

The transmitter may operate in one of eight data interface configurations as shown in Table 2. The compatibility configuration pin, COMPAT, establishes operation in either the "backplane" mode or the "Ethernet" compatible mode. The ten bit interface enable, TBIE, configuration input determines if the internal 8B/10B encoder will be used with uncoded input data or bypassed for a pre-encoded (coded) input data. The DDR configuration pin when enabled "reduces" the interface from an 8-/10-bit single data rate interface to a 4-/5-bit double data rate interface.

The configuration signals, TBIE and COMPAT, also affect the receiver's configuration.

Table 2. MC92603 Data Interface Modes

Data Interface Mode	COMPAT	TBIE	DDR
Backplane 8-bit Uncoded Data	Low	Low	Low
Backplane (4-bit reduced interface) Uncoded Data	Low	Low	High
Backplane 10-bit Coded Data	Low	High	Low
Backplane (5-bit reduced interface) Coded Data	Low	High	High
Ethernet compatible GMII	High	Low	Low
Ethernet compatible RGMII	High	Low	High
Ethernet compatible TBI	High	High	Low
Ethernet compatible RTBI	High	High	High

Transmit data is sampled and stored in the input FIFO on the rising edge (single data rate) of the appropriate transmit clock, if DDR is low, or both edges (double data rate) of the transmit clock if DDR is high. The FIFO accepts data to be transmitted and synchronizes it to the internal clock domain.

The transmitter data interface operates at high frequency (nominally 125MHz). In order to ease development of devices that interface with the Gigabit Ethernet transceivers, all transmitter data input interfaces are source synchronous. The data for each channel has its own dedicated clock input. This allows the clock at the source of the data to be routed with the data ensuring matched delay and timing. However, if per-channel clock sources are not available or deemed unnecessary, all channels may be clocked by a common clock source. The transceivers may be configured so that the channel A transmit clock is used as the source synchronous clock for all four channels. All transmitter clock inputs and the reference clock inputs must have identical frequencies, however, a phase shift of +/- 180^{o} is tolerated.

Backplane Application Modes (COMPAT = low)

Transmitting Uncoded Data - 8-/4-Bit Modes

The settings for the transmitter control signals when sending uncoded 8-bit or reduced interface 4-bit data is shown in Table 3.

When XMIT_x_ENABLE is low, an IDLE (K28.5) code group of proper running disparity is generated. The state of the XMIT_x_7-XMIT_x_0, XMIT_x_K, and XMIT_x_ERR signals are ignored. This allows the link to maintain alignment when transmission of data is not needed.

Table 3. Transmitter Control States for Uncoded Data (TBIE=low)

XMIT_x_ENABLE	XMIT_x_ERR	XMIT_x_K	Description
Low	Don't care	Don't care	Transmit IDLE (K28.5), ignore data inputs.
High	Low	Low	Transmit data present on data inputs.
High	Low	High	Transmit control data present on data inputs.
High	Low	High	Transmit disparity-style word synchronization event if the data inputs = AD (hex). The transmitter inputs will be ignored while sending these 16 code groups.
High	High	Don't care	Create an invalid 10 bit code group to be transmitted

When XMIT_x_ENABLE is high, uncoded data is presented in 8-/4-bit bytes to the input register through the XMIT_x_7 through XMIT_x_0 signals. The uncoded data is coded into 10-bit transmission code groups using an on-chip 8B/10B encoder. 8B/10B coding ensures DC balance across the link and sufficient transition density to facilitate reliable data and clock recovery. The XMIT_x_7 through XMIT_x_0 signals are interpreted as normal data when the XMIT_x_K signal is low.

The 8B/10B code set includes 12 special control codes. Special control codes may be transmitted by setting the XMIT_x_K high as indicated in Table 3. There are only 12 valid control code groups, if the data input is other than the 12 defined values then an illegal 10 bit code group will be generated and transmitted. This will be detected by the receiver as a "Code Error".

If XMIT_x_ERR is high then the 8B/10B encoder is forced to produce an invalid 10 bit code.

When using the device in a system where word alignment is required, it may be desirable to generate disparity-style word synchronization events. Also, it may be necessary to generate a disparity-style sync event for compatibility with legacy transceivers. A disparity style word synchronization event is generated by setting the transmit data inputs to a hex AD and XMIT_x_K high for the appropriate transmitter(s). The transmitter generates one of two unique 16-code group IDLE (K28.5) sequences depending on the current running disparity:

I+, I+, I-, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I- or

I-, I-, I+, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+, I-, I+

where I+ stands for IDLE of positive disparity, and I- stands for IDLE of negative disparity.

Transmitting Coded Data - 10-/5-Bit Modes

This operating mode is specified when the TBIE input is high. The state of COMPAT input does not affect the transmitter operation.

In this mode, ten-bit coded data may be transmitted, bypassing the internal 8B/10B encoder. The ten bits of data to transmit are presented on the XMIT_x_7 through XMIT_x_0 inputs with bits 9 and 8 on the XMIT_x_ERR and XMIT_x_ENABLE inputs, respectively.

When using the MC92603 or MC92604 in the backplane 10-bit, or reduced interface 5-bit mode, it is not necessary to use the 8B/10B code set, however, special care must be taken. The data must exhibit the same properties as 8B/10B coded data. DC balance must be maintained and there must be sufficient transition density to ensure reliable clock and data recovery at the receiver. If running in the Ethernet TBI or RTBI mode the data will be 8B/10B data. If the code used is NOT 8B/10B then it MUST support the K28.5 IDLE. The code also must be such to guarantee that no two codes when concatenated produce the 8 bit COMMA pattern.

The receivers require that COMMA code groups (K28.1, K28.5, or K28.7) be transmitted for byte synchronization. The 8-bit pattern ('00111110xx' or '11000001xx', ordered from bit 0 through 7) is used for alignment and link-to-link synchronization when operating in any of the byte or word synchronization modes. The pattern of code groups and data required to achieve word synchronization (available only in Backplane mode) depends on the configuration of the receiver. The appropriate sequence must be applied through the Ten/Five Bit Interface.

The XMIT_x_K signal is ignored by the transmitter in the backplane 10-/5-bit modes, however, it is used by the receiver.

Ethernet Compliant Applications Modes (COMPAT = high)

Transmitting Uncoded Data - GMII or RGMII Modes

When operating in the Ethernet compatibility mode, the MC92603/4 implements the Auto-Negotiation function at the PCS sublayer as defined in Clause 37 of **IEEE Std 802.3-2002.**

Auto-Negotiation Process

The transmitter enters auto-negotiate mode (if auto-negotiate is enabled) when one of 5 events occur.

- The part is reset.
- The part is requested to re-start the auto-negotiation process via the MDIO interface.
- The part is reconfigured via the MDIO interface.
- The associated receiver loses byte synchronization for more than 10 milliseconds.
- The associated receiver detects an auto-negotiate sequence initiated by its link partner.

When an auto-negotiate sequence is started, the transmitter initially sends at least 10 milliseconds of /C1/C2/ sequences with all zeroes as the Configuration Register contents. This forces the remote device to also enter auto-negotiate mode.

Then the contents of the Configuration Register are continuously sent until the associated receiver detects the same configuration being sent from the connected SERDES. The GEt is configured as full duplex 1 gigabit, therefore the configuration is as shown in Figure 3.

	15	14	13	12	11		9	8	7	6	5	4				0
Function	Next Page [1]	Ack [2]	RF2 [3]	RF1 [3]	Reserved			PS2[4]	PS1[4]	HD [5]	FD [6]	Reserved				
GEt Value	0	1/0	1/0	1/0	0	0	0	0	0	0	1	0	0	0	0	0

Figure 3. Configuration Register

1 Next Page - GEt does not support multiple pages of configuration Registers

2 Ack - is set when the receiver detects an identical configuration from the other transmitter

3 RF1 and RF2 - are “Remote Faults” as detected by the receiver

4 PS1 & PS2 - Are Pause Control features that are not supported by GEt

5 HD - GEt does not support Half Duplex mode

6 FD - GEt always runs in Full Duplex mode

The “Ack” bit is set when 3 consecutive matching Configuration Register values are received. The Auto-Negotiate state is complete when 3 consecutive matching Configuration Register values are received with the “Ack” bit set. The transmitter will continue sending Auto-Negotiate sequences once the Auto-Negotiate sequence is complete for at least 10 ms.

Data Transmission Process

Transmitter operation is controlled by the two input control signals XMIT_x_ENABLE and XMIT_x_ERR. When both XMIT_x_ENABLE and XMIT_x_ERR inputs are low the transmitter broadcasts IDLE Ordered_sets. Whenever a new series of IDLE Ordered_sets are started the first IDLE Ordered_set may be an I1 Ordered_set to correct the running disparity, all subsequent IDLE Ordered_sets will be I2s. The transmitter must be aware of even/oddness. K28.5 code groups are transmitted as the ‘even’ code group and either D5.6 or D16.2 as the ‘odd’ code group. This even/odd flag is set at initialization and must be maintained since other events will depend on this even/oddness.

When XMIT_x_ENABLE is raised, the data on the XMIT_x_7 through XMIT_x_0 inputs is assumed to be the first byte of an 8-byte preamble. The preamble usually consists of 7 consecutive 55 hex code groups followed by a D5 hex code group. The transmitter replaces the first 55 hex code group in the preamble with a /S/ Ordered_set to indicate Start_of_Frame. The MC92603/4 will support shorter preambles. The minimum preamble size is a single 55 (hex) code group followed by a D5 (hex) code group.

If XMIT_x_ERR is also raised when XMIT_x_ENABLE is raised then a false carrier is declared and a void code groups (/V/) is transmitted.

If XMIT_x_ERR is raised after XMIT_x_ENABLE has been raised **and** while data is being transferred this is a request to transmit an error propagation Ordered_set (/V/) for as many code groups as XMIT_x_ERR remains high.

When a normal End_of_Packet is detected (XMIT_x_ENABLE transitions to low and XMIT_x_ERR remains low) a single End_of_Packet ordered_set (/T/) is transmitted followed by at least one Carrier_Extend (/R/) ordered_set. A second Carrier_Extend will be inserted (if necessary) to complete an even/odd pair. This is then followed by IDLE ordered_sets to indicate the inter-packet gap. The first /I/ may be either an /I1/ or /I2/ depending upon running disparity.

If XMIT_x_ERR transitions to high as XMIT_x_ENABLE transitions to low this is defined as a ‘carrier extension.’ ‘Carrier extension’ is a half-duplex feature and is not supported in the MC92603/4. Therefore XMIT_x_ERR will be ignored while XMIT_x_ENABLE is low.

Transmitting Coded Data - TBI or RTBI Modes

The PMA sublayer of the 1000BASE-X specification does not require any functional differences in the transmitter from that used in the backplane application mode. Therefore, when operating in a mode specified when the TBIE input is high, the state of the COMPAT input does not affect the transmitter operation. See the previous 'backplane' section on transmitting coded data.

Receiver Functionality

The differential receiver recovers the serial transmitted data using an over-sampled transition tracking method. The recovered serial data is accumulated into ten-bit code groups. The ten-bit code groups are forwarded to the 8B/10B decoder and translated into the original 8-bit data. Alternately, the decoder can be bypassed and the ten-bit code group is forwarded to the receiver interface.

The code group or byte boundaries within the serial data stream are determined by aligning to COMMA (K28.1, K28.5, or K28.7) code groups. 'Byte' alignment is achieved when 4 COMMA code groups with the same alignment are detected.

The receiver also provides for word synchronization (this feature is available only in 'Backplane' operating modes). In this mode, all of the receivers are being used cooperatively to receive 32-bit (40 bit in TBI mode) words. Word synchronization assures that the receivers present the four bytes of a word simultaneously at the receiver output interface.

Interface Configuration

The receiver interface facilitates transfer of received data to the system. It also provides information on the status of the link. Table 4 describes the signals involved in the configuration of the receiver five operating modes.

Table 4. MC92603 Receiver Operating Modes (Common Features/Characteristics)

Operating Mode	BSYNC	COMPAT	TBIE
Backplane 10 or 5-bit Coded Data Modes - Non-aligned	Low	Low	High
Backplane 10 or 5-bit Coded Data Modes - Aligned	High	Low	High
Backplane 8 or 4-Bit Byte Modes	High	Low	Low
GMII or RGMII compatible Mode	High	High	Low
TBI or RTBI compatible Mode	High	High	High

The received data is presented on the RECV_x_7 through RECV_x_0 signals when operating in the GMII or 8-bit backplane modes. In the 10-bit backplane or TBI modes, RECV_x_ERR, RECV_x_DV become bits 9 and 8 respectively.

In the reduced interface modes the receiver signals RECV_x_7 through RECV_x_4 are not used and the 5th and 9th data bits are output on the RECV_x_DV signal.

The receiver status and error reporting is coded onto the RECV_x_ERR, RECV_x_DV, RECV_x_COMMA and RECV_x_K signals. Table 5 lists the description of the errors reported in the various receiver operational modes.

Table 5. Receiver Errors Reported for Receiver Modes

Description of Reported Errors	GMII/ RGMII	TBI/ RTBI	8-bit/ 4-bit	10-bit/ 5bit
Disparity Error: The 8B/10B decoder detected a disparity error.	YES	YES	YES	NO
Code Error: The 8B/10B decoder detected an illegal code group.	YES	NO	YES	NO
Overrun	YES	YES	YES	YES
Underrun	YES	YES	YES	YES
Not Word Sync: The receiver is byte synchronized but has not achieved or has lost word alignment and is searching for alignment.	NO	NO	YES	YES
Not Byte Sync: The receiver is in start-up or has lost byte alignment and is searching for alignment.	YES	YES	YES	YES

Data Alignment Configurations

Non-Aligned Mode (BSYNC = low)

In this mode no attempt is made to align the incoming data stream. The bits are simply accumulated into 10-bit code groups and forwarded. This mode should be used only with Backplane 10-/5-bit Data Mode (TBIE=high, COMPAT=low), and with Word Synchronization disabled (WSYNC1 & WSYNC0=low).

Byte-Aligned Mode (BSYNC = high)

The remaining 4 receiver operating modes align the incoming serial data into 10 bit code groups. At power-up, the receiver starts an alignment procedure, searching for the 8-bit pattern defined by the 8B/10B COMMA codes. Synchronization logic checks for the distinct sequence, '00111110xx' and '11000001xx' (ordered bit 0 to bit 7), characteristic of the three valid COMMA code groups. The search is done on the 10-bit data in the receiver, and is therefore independent of the state of TBIE or COMPAT. Alignment requires a minimum of four, error-free, received COMMA code groups to ensure proper alignment and lock. Non-COMMA code groups may be interspersed with the COMMA code groups. The disparity of the COMMA code groups is not important to alignment and can be positive, negative or any combination. The receiver begins to forward received code groups once locked on an alignment.

Word Synchronization

When the MC92603 is configured in either of the 'aligned backplane' modes (BSYNC high and COMPAT low), the four receivers can be used cooperatively to receive 32-bit (40-bit if TBIE is high) aligned word transfers. Word alignment is enabled by setting the word synchronization enable inputs, WSYNC1 or WSYNC0, high.

The word synchronization aligns code groups in the receiver's alignment FIFO. Synchronization is accomplished by lining up *word synchronization events* detected by each of the receivers, such that all are coincident at the same output stage of their FIFO.

Word synchronization events must be received at all concerned receivers within 40 bit-times of each other.

There are three word synchronization events as defined in Table 6.

Table 6. Word Synchronization Events

Word Synchronization Event	WSYNC1	WSYNC0
No word synchronization required	LOW	LOW
4 IDLE / 1 non-IDLE	LOW	HIGH
Disparity-based IDLE sequence	HIGH	LOW
Align to special control Character K28.3 (/A/)	HIGH	HIGH

Receiver Interface Timing Modes

The receiver interface is timed to the recovered clock or to the local reference clock, depending on the state of the recovered clock enable, RCCE, signal. RCCE set high enables timing relative to the recovered clock, set low enables timing relative to the reference clock. All receiver channels outputs are source synchronous. They may be configured to be source aligned or source centered with their respective RECV_x_CLK outputs.

Recovered Clock Timing Mode (RCCE = high)

When RCCE is set high, then RECV_REF_A is used to select the recovered clock to be used. If RECV_REF_A is high, then Channel A's recovered clock is used for all four channels. If it is low, then each channel uses its own recovered clock.

In order to track a transmitter frequency that is offset from the receiver's reference clock frequency, the duty cycle and period of the recovered clock is modulated. The recovered clock duty cycle may be reduced or increased by 200 ps (if nominal frequency is 125 Mhz) in order to match the transmitter frequency (if the reference clock frequency is 125mhz, this means that the minimum recovered clock cycle time is 7.8ns and the maximum recovered clock cycle is 8.2ns).

Reference Clock Timing Mode (RCCE = low)

Data is timed relative to the local reference clock when RCCE is low. Synchronization between the recovered clock and the reference clock is handled by the receiver interface. Frequency offset between the transmitter's reference clock and the receiver's reference clock causes overrun/underrun situations. Overrun occurs when the transmitter is running faster than the receiver. Underrun occurs when the transmitter is running slower than the receiver. The MC92603/4 performs rate adaption based on the context of the data streams to prevent over and under run situations.

In an overrun situation, data must be dropped in order to maintain synchronization between the clock domains. If add delete idle enable, ADIE, is high the receiver interface searches for the appropriate code groups to drop when overrun is imminent. If the appropriate code groups are not available to drop, receiver overrun may occur. When overrun occurs, the "Overrun" error is reported and data is dropped. Table 7 summarizes the rate adaption technique as a function of the receiver configuration when the receiver reference clock is slower than the transmitter reference clock.

Table 7. Receiver Reference clock is SLOWER than Transmitter Reference Clock

ADIE	COMPAT	Receive Mode	Result	Action Taken
Low	Low	N/A	Overrun	Two bytes of data are lost. First byte reports overrun, second byte is skipped.
High	Low	N/A	Data dropped	2 consecutive IDLEs (K28.5) are dropped.

Table 7. Receiver Reference clock is SLOWER than Transmitter Reference Clock (continued)

ADIE	COMPAT	Receive Mode	Result	Action Taken
High	High	Auto-Negotiate Sequence	Data dropped	16 bytes dropped (/C1/C2/C1/C2/)
High	High	IDLE Sequence	Data dropped	2 bytes dropped (/I2/)

In an underrun situation, data must be repeated in order to maintain synchronization between the clock domains. If ADIE is high the receiver interface repeats the appropriate code groups as described in Table 8 when underrun is imminent.

Table 8. Receiver Reference clock is FASTER than Transmitter Reference Clock

ADIE	COMPAT	Receive Mode	Result	Action Taken
Low	Low	N/A	Underrun	Two bytes of data are lost. First byte reports underrun, second byte repeats byte prior to underrun.
High	Low	N/A	Data repeated	2 consecutive IDLEs (K28.5) are repeated.
High	High	Auto-Negotiate Sequence	Data repeated	16 bytes repeated (/C1/C2/C1/C2/)
High	High	IDLE Sequence	Data repeated	2 bytes repeated (/I2/)

When operating in 'Word' mode all configured channels must add/delete IDLEs simultaneously. Therefore IDLEs must appear in the data stream for all channels simultaneously, so that IDLEs may be repeated or deleted.

The code group type and timing for rate adaption as described above, is determined by the current context of the packet stream. The data context is when the transceivers are transmitting MAC frames encapsulated into code group packets. The code groups in the packet can not be disturbed, therefore, rate adaption is accomplished in the IPG as previously described. A special case that must be considered in the data context is Jumbo frames.

Jumbo frames are not supported in the standard but are rather a de facto standard. Jumbo frames violate the untagged maximum frame size of 1518 code groups and increases the size to 16k code groups. Given a maximum total frequency offset of 200 ppm, a Jumbo frame could lead to a surplus or deficit of 1.67 code groups for which rate adaption must account. The depth of the receivers elastic buffers may be increased by configuring JPACK high in order to ensure against starvation in the presence of Jumbo frames. This increase will lead to longer receiver latency.

Gigabit Ethernet Compatible Operation

The operation of the transceivers in the Ethernet compatibility GMII and TBI modes and the correlation of the port signal names to the names in the **IEEE Std 802.3-2002** specification are listed in the following two sections.

GMII Interface

GMII Mode is enabled by setting the TBIE input low and COMPAT input high. When in this mode the receiver should be connected to a standard Gigabit Ethernet MAC as shown in Table 9.

Table 9. GMII Connection to Standard Ethernet MAC

IEEE 802.3_2002 Signal Name	Function	Direction (relative to GEt)	GEt Port Name
GTX_CLK	Transmit Clock	Input	XMIT_x_CLK
TX_EN	Transmit Enable	Input	XMIT_x_ENABLE
TX_ER	Force Error on Transmitted Byte	Input	XMIT_x_ERR
TXD<7:0>	Transmit Data	Input	XMIT_x_[7:0]
RX_CLK	Receive Clock	Output	RECV_x_CLK
RXD<7:0>	Receive Data	Output	RECV_x_[7:0]
RX_ER	Receiver has detected an error	Output	RECV_x_ERR
RX_DV	Receiver has detected data	Output	RECV_x_DV
MDC	Management Data Clock	Input	MD_CLK
MDIO	Management Data Input/Output	Bidirectional	MD_DATA
The following inputs must be externally pulled up/down as indicated			
Pull Up	Management Interface Enable	Input	MD_ENABLE
Variable (PUP/PUD)	MDIO PHY Address	Input	MD_ADR[4:2]
Pull Down	Disable unused Transmitter Input	Input	XMIT_x_K
Pull Down	Configuration Input - put in 8 bit mode	Input	TBIE
Pull Up	Configuration Input - put in synchronized mode	Input	BSYNC
Pull Down	Configuration Input - disable word alignment	Input	WSYNC1 & WSYNC0

Initially the receiver must attain byte alignment through the detection of 4 COMMA code groups with the same alignment as explained previously. Next the receiver must attain stream alignment per Figure 36-9 of '**IEEE Std 802.3-2002**.'

The RECV_x_ERR output remains high until both alignments are attained.

The receiver will now search for a Start_of_Packet code group (/S/). Upon the detection of a Start_of_Packet the receiver will replace that code group with a preamble code group (55 hex) and present this data on the receiver data output RECV_x_7 through RECV_x_0 as the RECV_x_DV output is raised. This is per Figures 36-7a and 36-7b of '**IEEE Std 802.3-2002**.'

Data will continue to be presented on the data outputs and the RECV_x_DV output will remain high until an End_of_Packet code group (/T/) is received. At this point the RECV_x_DV output will lowered and remain low until the next Start_of_Packet is received. When the End_of_Packet code group (/T/) is received the RECV_x_DV output will lowered after the previous data code group is presented on the receiver data interface (RECV_x_7 through RECV_x_0).

TBI Interface

TBI Mode is enabled by setting the TBIE and COMPAT inputs high. When in this mode, the MC92603 will conform to the **IEEE Std 802.3-2002** TBI interface signals and protocol. The complete TBI connection to a standard Ethernet MAC is show in Table 10.

Table 10. TBI Connection to Standard Ethernet MAC

802.3-2002 Signal	Function	Direction (relative to GEt)	GEt Port Name
PMA_TX_CLK	Transmit Clock	Input	XMIT_x_CLK
tx_code_group<9:0>	Transmit Data	Input	XMIT_x_ERR,XMIT_x_ENABLE,XMIT_x_[7:0]
EWRAP	Enable Data Wraparound	Input	XMIT_x_LBE
EN_CDET	Enable COMMA detect	Input	XMIT_x_K
COM_DET	Receiver Detected a COMMA	Output	RECV_x_COMMA
rx_code_group<9:0>	Receive Data	Output	RECV_x_ERR, RECV_x_DV, RECV_x_[7:0]
-LCK_REF	Enable Lock to Reference	Input	RCCE (normally low, affects all 4 channels)
PMA_RX_CLK<0:1>	Receive Clocks (both phases)	Output	RECV_x_CLK, $\overline{\text{RECV\_x\_CLK}}$
The following output is available but is not a standard TBI signal			
N/A	Receiver Detected an error	Output	RECV_x_K
The following inputs must be externally pulled up/down as indicated			
Pull Down	Management Interface Enable	Input	MD_ENABLE
Variable (PUP/PUD)	MDIO PHY Address	Input	MD_ADR[4:2]
Pull Up	Configuration	Input	TBIE
Pull Up	Configuration	Input	BSYNC

The receiver interface works similar to the backplane 10-bit mode except that word synchronization is not supported and non-aligned operation is not allowed. Also in this mode the XMIT_x_K input is not required for the transmitter so it is used to “enable COMMA detect”. The MC92603/4 will always initially perform even/odd alignment to the first IDLE (K28.5) code-group encountered. If XMIT_x_K is low it will NOT realign to any future IDLEs that may appear in the data stream. Data out of the receiver is even/odd aligned with the two output clocks. IDLEs (K28.5 code groups) are initially aligned with the rising edge of RECV_x_CLK_B. If “enable COMMA detect” is enabled (XMIT_x_K is high) then a data code group may be repeated to force this alignment if an IDLE is encountered in an ODD code group.

MDIO

The MDIO (Management Data Input/Output) interface as defined in Clause 22 of **IEEE Std 802.3-2002** is supported by the MC92603and MC92604 Gigabit Ethernet transceivers. Details for protocol and electrical characteristics are available in the standard.

The MC92603/4 chip MDIO interface consists of 1 enable input, 3 or 4 address inputs, one clock input, and one bidirectional data signal.

Some users may desire to use the MDIO interface, others may not. If the MDIO interface is to be used then the MD_ENABLE input must be tied high. The MDIO interface is available whether COMPAT is enabled or not. On power-up the MC92603/4 will always assume the default configuration defined by the pins of the device. The configuration can then be changed via the MDIO interface regardless of the application operating mode. If MDIO is not used (MD_ENABLE is low) The MC92603/4 will operate in the default configuration.

The MDIO interface is a multidrop serial interface and each part must have a unique PHY Address. In the MC92603 each channel is addressed separately. The base address to each transceiver must be mod 4. This address is read from three input ports that must be externally pulled up or pulled down to furnish a unique address for each part connected to a MDIO bus. The two least significant bits of the 5 bit address, are used

to uniquely identify each MC92603 channel (00 indicates Channel A, 01 = B, 10 = C, and 11 indicates Channel D (The least significant bit for the MC92604 determines channel A or B).

The 2.5 Mhz clock (MD_CLK) is sourced at the MDIO Master (MAC) and is used by each slave MDIO device. The MC92603/4 are designed as MDIO slave devices.

The MDIO data signal (MD_DATA) is a bidirectional serial signal used to read and write management data from/to the MDIO Registers.

The specification calls for up to 64 registers to be supported by MDIO. Some registers MUST be included as a minimum to meet the MDIO specification. These are identified as the “basic” register set. Other registers are optional and are considered part of the “extended” register set. The MC92603 and MC92604 have four sets of MDIO registers (1 per transceiver). Resisters for address 0 through 6 and 15 through 17, as defined in the specification, are fully supported. the registers 7 through 14 and 18 through 31 are NOT supported in the MC92603/4.

Test Features

TheMC92603 and MC92604 supports test modes for in-system BIST testing. They also has a five terminal JTAG interface as described in **IEEE Std 1149.1**.

Each channel of the transceiver may be individually configured for digital loop back where the transmitted data is looped back to its receiver independent of the receiver’s link inputs. The code groups transmitted are controlled by the normal transmitter controls. If the transceiver is working properly, the data/control code groups transmitted are received by the receiver. This allows system logic to use various data sequences to test the operation of the transceiver.

The loop-back signals are electrically isolated from the output signal pads. Therefore, if the outputs are shorted, or otherwise restricted, the loop-back signals still operate normally.

The receiver’s link input signals are also electrically isolated during loop back mode, such that their state does not affect the loop back path.

LBOE controls the state of the link output signals during Loop Back testing. If LBOE is low then XLINK_x_P/XLINK_x_N are held to low/high respectively. If LBOE is high then data will be present on the outputs.

The MC92603/4 has an integrated, 23rd order, Pseudo-Noise (PN) pattern generator. Stimulus from this generator may be used for system testing. The receiver, has a 23rd order signature analyzer that is synchronized to the incoming PN stream and may be used to count code group mismatch errors relative to the internal PN reference pattern. This implementation of the 23-bit PN generator and analyzer uses the polynomial: $f = 1 + x^5 + x^{23}$

The total mismatch error count is presented on the receiver interface signals and is reset to zero when BIST mode is entered. The count is updated continuously while in BIST mode. The value of this eight-bit error count is *sticky* in that the count will not wrap to zero upon overflow, but rather, stays at the maximum count value (11111111). In ALL BERT test modes an error counter is maintained in a MDIO Register for each specific channel.

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