EVALUATION KIT AVAILABLE

MAX8982A/MAX8982P/MAX8982X

Power-Management ICs for ICERA E400 Platform

General Description

The MAX8982A/MAX8982P/MAX8982X are complete power-management ICs for the latest LTE/WCDMA/GSM/GPRS/EDGE data card based on the new ICERA platform (E400). The MAX8982A operates from a 4.1V to 5.5V supply and contains four efficient step-down converters, nine low dropout linear regulators (LDOs) to power all RF and baseband circuitry, three current regulators with programmable current up to 24mA and embedded flash timers, and an I²C serial interface to program individual regulator output voltages as well as on/off control for flexibility. The linear regulators provide greater than 60dB PSRR, less than 45µV of output noise, and minimal cross coupling noise between LDOs.

The MAX8982X/MAX8982P operates from a 2.9V to 5.5V supply. The MAX8982X has the same features as the MAX8982A, except it does not have BUCK3, BUCK4, and LDO8. The MAX8982P has the same features as the MAX8982A.

All buck converters and LDOs are enabled/disabled by either I²C or PWR_REQ control signal after power-up. This feature provides more flexibility in system design.

Applications

GSM, GPRS, EDGE, WCDMA, and LTE
Data Card with New ICERA Platform (E400)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8982AEWO+T	-40°C to +85°C	42 WLP
MAX8982PEWO+T	-40°C to +85°C	42 WLP
MAX8982XEWO+T	-40°C to +85°C	42 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel. These devices have a minimum order increment of 1k pieces.

Features

- **4 High-Efficiency Buck Converters**
  - **0.9V at 1.2A (1.3 for MAX8982P) for CORE with DVS Function (0.6V to 1.2V in 25mV Steps) and Slew Rate Control**
  - **1.8V at 600mA for System IO**
  - **3.2V at 600mA for All LDO Inputs (2.9V to 3.65V in 50mV Steps) (MAX8982A/MAX8982P Only)**
  - **3.4V at 1.8A for GSM/WCDMA PA (3.0V to 3.75V in 50mV Steps) (MAX8982A/MAX8982P Only)**
- **9 LDO Linear Regulators**
  - **2.7V at 300mA on LDO1 for RF Transceiver**
  - **1.8V at 150mA on LDO2 for RF Transceiver**
  - **2.8V at 150mA on LDO3 for Analogue BB**
  - **0.9V at 50mA on LDO4 for BB PLL with the Separate Input for a Higher Efficiency**
  - **3.0V at 150mA on LDO5 for SD Card**
  - **2.7V at 150mA on LDO6 for TCXO**
  - **1.8V or 3.0V at 150mA on LDO7 for SIM**
  - **3.0V at 150mA on LDO8 for USB with the Separate Input (MAX8982A/MAX8982P Only)**
  - **0.9V at 50mA on LDO9 for BB with the Separate Input for a Higher Efficiency**
- **32 Programmable Voltage Options and External Input on BUCK1 (0.9V Default) for DVS**
- **16 Programmable Voltage Options for BUCK3 (MAX8982A/MAX8982P Only)**
- **16 Programmable Voltage Options on BUCK4 (MAX8982A/MAX8982P Only)**
- **Programmable Voltage Options for All LDOs (LDO8 for MAX8982A/MAX8982P Only)**
- **BUCK2, BUCK3 (MAX8982A/MAX8982P Only), LDO3, and Internal 32kHz Clock Default On at Initial Startup**
- **All Buck Converters and LDOs are Enabled by Either I²C or Power Request Control (PWR_REQ) After Power-Up**
- **3 Current Regulators with 8 Dimming Current Options Up to 24mA with Embedded Flash Timer**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5472; Rev 2; 4/11

MAX8982A/MAX8982P/MAX8982X

Power-Management ICs for ICERA E400 Platform

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ABSOLUTE MAXIMUM RATINGS

V_{DDA}, V_{DDB}, IN4, IN1A, IN1B to GND.....-0.3V to +6V
REFBP, BUCK1, BUCK2, BUCK3, BUCK4,
EN to GND.....-0.3V to (V_{IN1A}, V_{IN1B} + 0.3V)
SDA, SCL, PWR_REQ, DVS1, $\overline{IRQ}$, $\overline{RESET}$, IN3,
N32kHz to GND..... -0.3V to (V_{BUCK2} + 0.3V)
OUT1, OUT2 to GND ..... -0.3V to (V_{DDA} + 0.3V)
OUT3, OUT5, OUT6, VSIM to GND ..... -0.3V to (V_{DDB} + 0.3V)
OUT8 to GND.....-0.3V to (V_{IN4} + 0.3V)
OUT4, OUT9 to GND .....-0.3V to (V_{IN3} + 0.3V)
PGND1, PGND2, PGND3, PGND4 to GND .....-0.3V to +0.3V
DR1, DR2, DR3 to GND .....-0.3V to ($V_{IN1\_}$ + 0.3V)
LX1 Continuous Current (Note 1).....1200mA
LX2, LX3 Continuous Current (Note 1) 600mA
LX4 Continuous Current (Note 1).....1800mA
Continuous Power Dissipation (T_A = +70°C)
7 x 6 42-Bump WLP, 0.5mm Pitch, 3.75mm x 3.20mm
(derate 27.8mW/°C above +70°C).....2.22W
Operating Temperature Range..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Note 1: LX1–LX4 have internal clamp diodes to PGND_, IN1A, and IN1B. Applications that forward bias this diode should take care not to exceed the power dissipation limits of the device.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

GENERAL ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = +5.0V and $C_{OUT1,2,3+CIN\_}$ = 1000µF, MAX8982X: V_{IN1A} = V_{IN1B} = +3.3V and $C_{OUT1,2,3+CIN\_}$ = 20µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN1A, IN1B, IN4 ESD Protection	Module level ESD protection, in-circuit tested with 0.1µF ceramic capacitor		±10		kV
Shutdown Supply Current (Note 4)	EN = GND			10	µA
No Load Supply Current	MAX8982A/MAX8982P, V_{EN} = $V_{IN1\_}$, BUCK3 and OUT3 on (default output), all other regulators off		300		µA
	MAX8982X, V_{EN} = $V_{IN1\_}$, OUT3 on (default output), all other regulators off		300		
	MAX8982A/MAX8982P, V_{EN} = $V_{IN1\_}$, BUCK1 on (default output), BUCK2 on (default output), BUCK3 on (default output), all LDOs (except LDO8) default output on		600		
	MAX8982X, V_{EN} = $V_{IN1\_}$, BUCK1 on (default output), BUCK2 on (default output), all LDOs (except LDO8) default output on		600		
Loaded Supply Current	MAX8982A/MAX8982P, V_{EN} = $V_{IN1\_}$, 32kHz clock on, BUCK2 on (default output) with 200µA load, BUCK3 on (default output), OUT3 on (default output) with 20µA load, OUT2 on (default output) with 100µA load, V_{VSIM} = 3.0V with 50µA load, OUT8 on (default output) with 100µA load		1000		µA
	MAX8982X, V_{EN} = $V_{IN1\_}$, 32kHz clock on, BUCK2 on (default output) with 200µA load, OUT3 on (default output) with 20µA load, OUT2 on (default output) with 100µA load, V_{VSIM} = 3.0V with 50µA load		1000		

GENERAL ELECTRICAL CHARACTERISTICS (continued)

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = +5.0V and $C_{OUT1,2,3+CIN\_}$ = 1000µF, MAX8982X: V_{IN1A} = V_{IN1B} = +3.3V and $C_{OUT1,2,3+CIN\_}$ = 20µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING VOLTAGE					
IN1A, IN1B Operating Voltage	MAX8982A	4.1		5.5	V
	MAX8982X/MAX8982P	2.9		5.5	
Undervoltage Lockout	MAX8982A, $V_{IN1\_}$ rising	3.5	3.8	4.1	V
	MAX8982A, $V_{IN1\_}$ falling		3.5		
	MAX8982X/MAX8982P, $V_{IN1\_}$ rising	2.5	2.7	2.9	
	MAX8982X/MAX8982P, $V_{IN1\_}$ falling		2.4		
OVERVOLTAGE LOCKOUT (OVP)					
Overvoltage Lockout (Shutdown All Outputs Including LDO7)	$V_{IN1\_}$ rising		5.75	5.93	V
IN1A, IN1B Overvoltage Hysteresis			250		mV
THERMAL SHUTDOWN					
Threshold	T_J rising		160		°C
Hysteresis			10		°C
HOT TEMPERATURE DETECTION					
Threshold	Interrupt enabled, T_J rising, typical hysteresis = +10°C		+125		°C
REFERENCE					
REFBP Output Voltage	$0 \le I_{REFBP} \le 1µA$	0.788	0.80	0.812	V
Supply Rejection	$4.1V \le V_{IN1\_} \le 5.5V$		0.2		mV
LOGIC AND CONTROL INPUTS (SDA, SCL, EN, DVS1, PWR_REQ)					
Input Low Level	T_A = +25°C			0.3	V
Input High Level	T_A = +25°C	1.2			V
Logic Input Current	$0V < V_{IN1\_} < 5.5V$, T_A = +25°C	-1		+1	µA
	$0V < V_{IN1\_} < 5.5V$, T_A = +85°C		0.1		
LOGIC AND CONTROL OUTPUTS					
SDA Output Low Level	I_{SDA} = 6mA			0.4	V
I²C INTERFACE (V_{SCL} = V_{SDA} = 1.8V, Note 2, Figure 16)					
Clock Frequency				400	kHz
Bus Free Time Between START and STOP (t_{BUF})		1.3			µs
Hold Time Repeated START Condition (t_{HD_STA})		0.6			µs
SCL Low Period (t_{LOW})		1.3			µs
SCL High Period (t_{HIGH})		0.6			µs
Setup Time Repeated START Condition (t_{SU_STA})		0.6			µs
SDA Hold Time (t_{HD_DAT})		0			µs
SDA Setup Time (t_{SU_DAT})		100			ns

GENERAL ELECTRICAL CHARACTERISTICS (continued)

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = +5.0V and $C_{OUT1,2,3+CIN\_}$ = 1000µF, MAX8982X: V_{IN1A} = V_{IN1B} = +3.3V and $C_{OUT1,2,3+CIN\_}$ = 20µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of Both SDA and SCL Signals			50		ns
Setup Time for STOP Condition (t_{SU_STO})		0.6			µs

BUCK1 ELECTRICAL CHARACTERISTICS

(MAX8982AMAX8982P: V_{IN1A} = V_{IN1B} = +5.0V and $C_{OUT1,2,3+CIN\_}$ = 1000µF, MAX8982X: V_{IN1A} = V_{IN1B} = +3.3V and $C_{OUT1,2,3+CIN\_}$ = 20µF, C_{REFBP} = 0.1µF, C_{OUT} = 10µF, L = 2.2µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (Note 4)	No load, no switching			65		µA
Default Output Voltage	I_{LOAD} = 100mA		0.873	0.9	0.927	V
Output Voltage Accuracy	I_{LOAD} = 100mA, V_{BUCK1} tested at 0.6V, 0.775V, 1V, 1.2V in production (0.6V to 1.2V in 25mV steps)		-3		+3	%
Maximum Output Current	V_{BUCK1} = 0.9V, T_A = +25°C	MAX8982A/MAX8982X	1200			mA
		MAX8982P	1300			
Current Limit	pFET switch (MAX8982A/MAX8982X)		1400	1800	2500	mA
	pFET switch (MAX8982P)		1500	1900	2600	
	nFET rectifier (MAX8982A/MAX8982X)		1000	1400	1900	
	nFET rectifier (MAX8982P)		1100	1500	2000	
On-Resistance	pFET switch, I_{LX1} = -150mA			0.3		Ω
	nFET rectifier, I_{LX1} = 150mA			0.15		
Ramp-Up/Down Rate Control	Same for both up and down	RASD1[0:1] = 00		5		mV/µs
		RASD1[0:1] = 01		10		
		RASD1[0:1] = 10		12.5 (default)		
		RASD1[0:1] = 11		25		
Rectifier Off Current Threshold				40		mA
Minimum On-Time	t_{ON}			40		ns
Minimum Off-Time	t_{OFF}			40		ns
Efficiency (Note 4)	V_{BUCK1} = 0.9V, I_{LOAD} = 400mA			85		%
Shutdown Output Resistance (Active Discharge Resistance)	I^2C programmable, default OFF			1		kΩ
Output Load Regulation	Equal to inductor DC resistance divided by 4			R_L/4		V/A

BUCK2 ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = +5.0V and $C_{OUT1,2,3+CIN\_}$ = 1000µF, MAX8982X: V_{IN1A} = V_{IN1B} = +3.3V and $C_{OUT1,2,3+CIN\_}$ = 20µF, C_{REFBP} = 0.1µF, C_{OUT} = 2.2µF, L = 1µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 4)	No load, no switching		26		µA
Output Voltage	I_{LOAD} = 100mA	1.746	1.8	1.854	V
Output Current	V_{BUCK2} = 1.8V, T_A = +25°C	600			mA
Current Limit	pFET switch	700	1100	1500	mA
	nFET rectifier	500	750	1200	
On-Resistance	pFET switch, I_{LX2} = -150mA		0.65		Ω
	nFET rectifier, I_{LX2} = 150mA		0.3		
Rectifier Off Current Threshold			40		mA
Minimum On-Time	t_{ON}		70		ns
Minimum Off-Time	t_{OFF}		70		ns
Efficiency (Note 4)	V_{BUCK2} = 1.8V, I_{LOAD} = 250mA		85		%
Shutdown Output Resistance (Active Discharge Resistance)	I^2C programmable, default ON		100		Ω
Output Load Regulation	Equal to inductor DC resistance divided by 4		R_L/4		V/A

BUCK3 ELECTRICAL CHARACTERISTICS

(MAX8982A/MX8982P only, V_{IN1A} = V_{IN1B} = +5.0V, $C_{OUT1,2,3+CIN\_}$ = 1000µF, C_{REFBP} = 0.1µF, C_{OUT} = 2.2µF, L = 2.2µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 4)	No load, no switching		40		µA
Default Output Voltage	I_{LOAD} = 100mA	3.10	3.2	3.29	V
Programmable Output Voltage	I_{LOAD} = 100mA, programmable output voltage step = 50mV		2.90		V
			2.95		
			3.00		
			3.05		
			3.10		
			3.15		
			3.20		
			3.25		
			3.30		
			3.35		
			3.40		
			3.45		
			3.50		
			3.55		
			3.60		
			3.65		
Maximum Output Current	V_{BUCK3} = 3.2V, T_A = +25°C	600			mA
Efficiency (Note 4)	V_{BUCK3} = 3.2V, I_{LOAD} = 300mA		90		%

BUCK3 ELECTRICAL CHARACTERISTICS (continued)

(MAX8982A/MAX8982P only, V_{IN1A} = V_{IN1B} = +5.0V, $C_{OUT1,2,3+CIN\_}$ = 1000µF, C_{REFBP} = 0.1µF, C_{OUT} = 2.2µF, L = 2.2µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit	pFET switch	700	1100	1500	mA
	nFET rectifier	500	750	1200	
On-Resistance	pFET switch, I_{LX3} = -150mA		0.65		Ω
	nFET rectifier, I_{LX3} = 150mA		0.3		
Rectifier Off Current Threshold			80		mA
Minimum On-Time	t_{ON}		70		ns
Minimum Off-Time	t_{OFF}		70		ns
Shutdown Output Resistance (Active Discharge Resistance)	I^2C programmable, default off		1		kΩ

BUCK4 ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P only, V_{IN1A} = V_{IN1B} = +5.0V, $C_{OUT1,2,3+CIN\_}$ = 1000µF, C_{REFBP} = 0.1µF, C_{OUT} = 20µF, L = 1µH, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Default Output Voltage	I_{LOAD} = 100mA	3.298	3.40	3.502	V
Programmable Output Voltage	I_{LOAD} = 100mA, programmable output voltage step = 50mV		3.00		V
			3.05		
			3.10		
			3.15		
			3.20		
			3.25		
			3.30		
			3.35		
			3.40		
			3.45		
			3.50		
			3.55		
			3.60		
			3.65		
			3.70		
			3.75		
Efficiency (Note 4)	V_{BUCK4} = 3.4V, I_{LOAD} = 500mA		90		%
Maximum Output Current		1800			mA
p-Channel On-Resistance	I_{LX4} = 150mA		100		mΩ
n-Channel On-Resistance	I_{LX4} = 150mA		100		mΩ
p-Channel Current-Limit Threshold			2700		mA
n-Channel Negative Current Limit			1500		mA
Maximum Duty Cycle			100		%
Minimum Duty Cycle			16.5		%
PWM Frequency	f_{OSC}	1.8	2.0	2.2	MHz
Shutdown Output Resistance (Active Discharge Resistance)	I^2C programmable, default off		1		kΩ

OUT1 (LDO1) ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{DDA} = +3.2V and $C_{VDD\_}$ = 10µF, MAX8982X: V_{DDA} = +3.3V and $C_{VDD\_}$ = 20µF, C_{REFBP} = 0.1µF, C_{OUT1} = 4.7µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Default Output Voltage	I_{LOAD} = 50mA	2.619	2.70	2.781	V
Maximum Output Current		300			mA
Current Limit (Note 4)	V_{OUT1} = 90% of its regulation	310	550	940	mA
Dropout Voltage (Note 4)	I_{LOAD} = 200mA, T_A = +85°C		50	100	mV
Line Regulation	2.9V ≤ V_{DDA} ≤ 3.65V, I_{LOAD} = 150mA		2.4		mV
Load Regulation	1mA < I_{LOAD} < 300mA		12		mV
Transient Response	di/dt = I_{MAX}/0.1µs, 1kHz < 1/T < 0.5MHz, where T is the period of step load, 1mA to 300mA		50		mV
Power-Supply Rejection $\Delta V_{OUT}/\Delta V_{IN}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA		60		dB
Output Noise Voltage	100Hz to 100kHz, I_{LOAD} = 30mA		45		μV_{RMS}
Programmable Output Voltages	I_{LOAD} = 50mA		2.65		V
			2.70		
			2.75		
			2.80		
			2.85		
			2.90		
			2.95		
			3.00		
Startup Time from Shutdown (Note 4)	I_{LOAD} = 300mA		40	100	µs
Startup Transient Overshoot (Note 4)	I_{LOAD} = 300mA		3	50	mV
Shutdown Output Impedance (Active Discharge Resistance)	I^2C programmable, default off		100		Ω

OUT2 (LDO2) ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{DDA} = +3.2V and $C_{VDD\_}$ = 10µF, MAX8982X: V_{DDA} = +3.3V and $C_{VDD\_}$ = 20µF, C_{REFBP} = 0.1µF, C_{OUT2} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Default Output Voltage	I_{LOAD} = 50mA	1.746	1.80	1.854	V
Maximum Output Current		150			mA
Current Limit (Note 4)	V_{OUT2} = 90% of its nominal regulation voltage	165	360	650	mA
Dropout Voltage (Note 4)	I_{LOAD} = 100mA, T_A =+85°C		150	300	mV
Line Regulation	2.9V ≤ V_{DDA} ≤ 3.65V, I_{LOAD} = 100mA		2.4		mV
Load Regulation	50µA < I_{LOAD} < 150mA		25		mV
Power-Supply Rejection $\Delta V_{OUT}/\Delta V_{IN}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA		60		dB
Output Noise Voltage	100Hz to 100kHz, I_{LOAD} = 30mA		45		μV_{RMS}

OUT2 (LDO2) ELECTRICAL CHARACTERISTICS (continued)

(MAX8982A/MAX8982P: V_{DDA} = +3.2V and $C_{VDD\_}$ = 10µF, MAX8982X: V_{DDA} = +3.3V and $C_{VDD\_}$ = 20µF, C_{REFBP} = 0.1µF, C_{OUT2} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Programmable Output Voltages	I_{LOAD} = 50mA		1.50		V
			1.80		
			2.70		
			1.70		
Startup Time from Shutdown (Note 4)	I_{LOAD} = 150mA		40	100	µs
Startup Transient Overshoot (Note 4)	I_{LOAD} = 150mA		3	50	mV
Shutdown Output Impedance (Active Discharge Resistance)	I^2C programmable, default off		100		Ω

OUT3 (LDO3) ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{DDB} = +3.2V and $C_{VDD\_}$ = 10µF, MAX8982X: V_{DDB} = +3.3V and $C_{VDD\_}$ = 20µF, C_{REFBP} = 0.1µF, C_{OUT3} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Default Output Voltage	I_{LOAD} = 50mA	2.716	2.800	2.884	V
Maximum Output Current		150			mA
Current Limit (Note 4)	V_{OUT3} = 90% of its regulation	165	360	650	mA
Dropout Voltage	I_{LOAD} = 100mA, T_A = +85°C		150	300	mV
Line Regulation	3.2V ≤ V_{DDB} ≤ 3.65V, I_{LOAD} = 100mA		2.4		mV
Load Regulation	50µA < I_{LOAD} < 150mA		25		mV
Power-Supply Rejection $\Delta V_{OUT}/\Delta V_{IN}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA		60		dB
Output Noise Voltage	100Hz to 100kHz, I_{LOAD} = 30mA		45		μV_{RMS}
Programmable Output Voltage	I_{LOAD} = 50mA		2.65		V
			2.70		
			2.75		
			2.80		
			2.85		
			2.90		
			2.95		
			3.00		
Startup Time from Shutdown (Note 4)	I_{LOAD} = 150mA			100	µs
Startup Transient Overshoot (Note 4)	I_{LOAD} = 150mA			50	mV
Shutdown Output Impedance (Active Discharge Resistance)	I^2C programmable, default off		100		Ω

OUT4 (LDO4) ELECTRICAL CHARACTERISTICS

(MAX8982_: V_{IN3} = V_{BUCK2} = 1.8V, C_{IN3} = 2.2µF, C_{REFBP} = 0.1µF, C_{OUT4} = 2.2µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Default Output Voltage	I_{LOAD} = 10mA	0.873	0.9	0.927	V
Maximum Output Current		50			mA
Current Limit (Note 4)	V_{OUT4} = 90% of its regulation	55	120	220	mA
Load Regulation	50µA < I_{LOAD} < 10mA		25		mV
Power-Supply Rejection $\Delta V_{OUT}/\Delta V_{IN}$	f = 10Hz to 10kHz, I_{LOAD} = 10mA		60		dB
Output Noise Voltage	100Hz to 100kHz, I_{LOAD} = 10mA		45		μV_{RMS}
Programmable Output Voltage	I_{LOAD} = 10mA		0.80		V
			0.90		
			1.00		
			1.10		
			1.20		
Startup Time from Shutdown (Note 4)	I_{LOAD} = 50mA			100	µs
Startup Transient Overshoot (Note 4)	I_{LOAD} = 50mA			50	mV
Shutdown Output Impedance (Active Discharge Resistance)	I^2C programmable, default off		100		Ω

OUT5 (LDO5) ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{DDB} = +3.2V and $C_{VDD\_}$ = 10µF, MAX8982X: V_{DDB} = +3.3V and $C_{VDD\_}$ = 20µF, C_{REFBP} = 0.1µF, C_{OUT5} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Default Output Voltage	I_{LOAD} = 50mA	2.91	3.00	3.09	V
Maximum Output Current		150			mA
Current Limit (Note 4)	V_{OUT5} = 90% of its regulation	165	360	650	mA
Dropout Voltage (Note 4)	I_{LOAD} = 100mA, T_A = +85°C		150	300	mV
Line Regulation	3.2V ≤ V_{DDB} ≤ 3.65V, I_{LOAD} = 100mA		2.4		mV
Load Regulation	50µA < I_{LOAD} < 150mA, V_{OUT} = 2.8V		25		mV
Power-Supply Rejection $\Delta V_{OUT}/\Delta V_{IN}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA		60		dB
Output Noise Voltage	100Hz to 100kHz, I_{LOAD} = 30mA		45		μV_{RMS}
Programmable Output Voltage	I_{LOAD} = 50mA, V_{DDB} = 3.4V for V_{OUT} = 3.2V		2.80		V
			2.90		
			3.00		
			3.20		
Startup Time from Shutdown (Note 4)	I_{LOAD} = 150mA			100	µs
Startup Transient Overshoot (Note 4)	I_{LOAD} = 150mA			50	mV
Shutdown Output Impedance (Active Discharge Resistance)	I^2C programmable, default off		100		Ω

OUT6 (LDO6) ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{DDB} = +3.2V and $C_{VDD\_}$ = 10µF, MAX8982X: V_{DDB} = +3.3V and $C_{VDD\_}$ = 20µF, C_{REFBP} = 0.1µF, C_{OUT6} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Default Output Voltage	I_{LOAD} = 50mA	2.619	2.70	2.781	V
Maximum Output Current		150			mA
Current Limit (Note 4)	V_{OUT6} = 90% of its regulation	165	360	650	mA
Dropout Voltage (Note 4)	I_{LOAD} = 100mA, T_A = +85°C		150	300	mV
Line Regulation	2.90V ≤ V_{DDB} ≤ 3.65V, I_{LOAD} = 100mA		2.2		mV
Load Regulation	50µA < I_{LOAD} < 150mA		25		mV
Power-Supply Rejection $\Delta V_{OUT}/\Delta V_{IN}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA		60		dB
Output Noise Voltage	100Hz to 100kHz, I_{LOAD} = 30mA		45		μV_{RMS}
Programmable Output Voltage	I_{LOAD} = 50mA		2.65		V
			2.70		
			2.75		
			2.80		
			2.85		
			2.90		
			2.95		
			3.00		
Startup Time from Shutdown (Note 4)	I_{LOAD} = 150mA			100	µs
Startup Transient Overshoot (Note 4)	I_{LOAD} = 150mA			50	mV
Shutdown Output Impedance (Active Discharge Resistance)	I^2C programmable, default off		100		Ω

VSIM (LDO7) ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{DDB} = +3.2V and $C_{VDD\_}$ = 10µF, MAX8982X: V_{DDB} = +3.3V and $C_{VDD\_}$ = 20µF, C_{REFBP} = 0.1µF, C_{OUT} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	50µA < I_{LOAD} < 20mA, 1.8V mode	1.746	1.80	1.854	V
	50µA < I_{LOAD} < 20mA, 3.0V mode (default)	2.91	3.00	3.09	
Maximum Output Current	2.9V ≤ V_{DDB} ≤ 3.65V, 1.8V mode	150			mA
Current Limit (Note 4)	V_{VSIM} = 90% of 1.8V mode	165	360	650	mA
Dropout Voltage (Note 4)	I_{LOAD} = 20mA, 3V mode		120	200	mV
Line Regulation	2.9V ≤ V_{DDB} ≤ 3.65V, I_{LOAD} = 50µA (1.8V mode)		0.1		mV
Load Regulation	50µA < I_{LOAD} < 20mA (1.8V mode)		25		mV
Power-Supply Rejection	f = 10kHz, I_{LOAD} = 10mA		57		dB
Output Noise Voltage	100Hz to 100kHz, I_{LOAD} = 10mA		80		µV
VSIM Discharge Resistance (Active Discharge Resistance)	I^2C programmable, default off		100		Ω

OUT8 (LDO8) ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P only, V_{IN4} = $V_{IN1\_}$ = +5.0V, C_{IN4} = 1.0µF, C_{REFBP} = 0.1µF, C_{OUT8} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Input Operating Range	Guaranteed by output voltage accuracy	3.0		5.5	V
Overvoltage Lockout (Shutdown LDO8 Output)	V_{IN4} rising, $V_{IN1\_}$ = V_{IN4}		5.75	5.93	V
Overvoltage Hysteresis			250		mV
Default Output Voltage	I_{LOAD} = 50mA	2.91	3.00	3.09	V
Maximum Output Current		150			mA
Current Limit (Note 4)	V_{OUT8} = 90% of its regulation	165	360	650	mA
Dropout Voltage (Note 4)	100mA, T_A = +85°C		150	300	mV
Line Regulation	3.4V ≤ V_{IN4} ≤ 5.5V, V_{OUT8} = 3.1V, I_{LOAD} = 100mA		2.2		mV
Load Regulation	50µA < I_{LOAD} < 150mA		25		mV
Power-Supply Rejection $\Delta V_{OUT}/\Delta V_{IN}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA		60		dB
Output Noise Voltage (RMS)	100Hz to 100kHz, I_{LOAD} = 30mA		45		μV_{RMS}
Programmable Output Voltage	I_{LOAD} = 50mA		3.00		V
			3.10		
			3.20		
			3.30		
Startup Time from Shutdown (Note 4)	I_{LOAD} = 150mA			100	µs
Startup Transient Overshoot (Note 4)	I_{LOAD} = 150mA			50	mV
Shutdown Output Impedance (Active Discharge Resistance)	I^2C programmable, default off		100		Ω

OUT9 (LDO9) ELECTRICAL CHARACTERISTICS

(MAX8982_: V_{IN3} = V_{BUCK2} = 1.8V, C_{IN3} = 2.2µF, C_{REFBP} = 0.1µF, C_{OUT9} = 2.2µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Default Output Voltage	±I_{LOAD} = 10mA, V_{IN3} = 1.8V	0.873	0.900	0.927	V
Maximum Output Current		50			mA
Current Limit (Note 4)	V_{OUT9} = 90% of its regulation	55	120	220	mA
Load Regulation	50µA < I_{LOAD} < 50mA		25		mV
Power-Supply Rejection $\Delta V_{OUT}/\Delta V_{IN}$	f = 10Hz to 10kHz, I_{LOAD} = 10mA		60		dB
Output Noise Voltage	100Hz to 100kHz, I_{LOAD} = 10mA		45		μV_{RMS}
Programmable Output Voltage	I_{LOAD} = 10mA		0.80		V
			0.90		
			1.00		
			1.10		
			1.20		
Startup Time from Shutdown (Note 4)	I_{LOAD} = 50mA			100	µs

OUT9 (LDO9) ELECTRICAL CHARACTERISTICS (continued)

(MAX8982_: V_{IN3} = V_{BUCK2} = 1.8V, C_{IN3} = 2.2µF, C_{REFBP} = 0.1µF, C_{OUT9} = 2.2µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Startup Transient Overshoot (Note 4)	I_{LOAD} = 50mA			50	mV
Shutdown Output Impedance (Active Discharge Resistance)	I^2C programmable, default off		100		Ω

$\overline{\text{RESET}}$ ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = +5V, MAX8982X: V_{IN1A} = V_{IN1B} = +3.3V, V_{BUCK2} = 1.8V, C_{BUCK2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output High Voltage	Internal logic supply I_{SOURCE} = 0µA	V_{BUCK2} - 0.3V			V
Output Low Voltage	Internal logic supply I_{SINK} = 500µA			0.3	V
$\overline{\text{RESET}}$ Enabled (Note 4)	From BUCK2 enable (Figure 4)		625		µs
$\overline{\text{RESET}}$ Disabled (Note 4)	With respect to $\overline{\text{IRQ}}$ = low	26		78	µs
Pullup Resistance to BUCK2		8	14	22	kΩ

$\overline{\text{IRQ}}$ ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = +5.0V, MAX8982X: V_{IN1A} = V_{IN1B} = +3.3V, V_{BUCK2} = 1.8V, C_{BUCK2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise specified.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output High Voltage	Internal logic supply I_{SOURCE} = 0µA	V_{BUCK2} - 0.3V			V
Output Low Voltage	Internal logic supply I_{SINK} = 500µA			0.3	V
Pullup Resistance to BUCK2		100	200	400	kΩ

CURRENT REGULATOR ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = +5V and $V_{DD\_}$ = 3.2V, MAX8982X: V_{IN1A} = V_{IN1B} = +3.3V and $V_{DD\_}$ = 3.3V, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
DR_ Sink Current Range		3		24	mA
DR_ Current Sink Programmable	DR_[2:0] = 000		3		mA
	DR_[2:0] = 001		6		
	DR_[2:0] = 010		9		
	DR_[2:0] = 011		12		
	DR_[2:0] = 100		15		
	DR_[2:0] = 101		18		
	DR_[2:0] = 110		21		
	DR_[2:0] = 111 (default)		24		
DR_ Sink Current Accuracy (Note 4)	T_A = +25°C	-10		+10	%
	T_A = -40°C to +85°C	-15		+15	
$V_{DR\_}$ Voltage Drop	$I_{DR\_}$ = 24mA		60	120	mV

FLASH TIMER ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: $V_{IN1A} = V_{IN1B} = +5V$ and $V_{DD\_} = +3.2V$, MAX8982X: $V_{IN1A} = V_{IN1B} = +3.3V$ and $V_{DD\_} = +3.3V$, $C_{REFBP} = 0.1\mu F$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 4, Figure 11)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Flash Timer Resolution			25		ms
Pattern Period, t_P	7-bit programmable in 25ms steps	0	0 (0000000) 25 (0000001) 50 75 . . 3175 (1111111)	3175	ms
Number of Programmable On Threshold			4		
Time for Flash to Turn On, t_1	7-bit programmable in 25ms steps	0	0 (0000000) 25 (0000001) 50 . . 3175 (1111111)	3175	ms
Time for Flash to Turn On, t_2	7-bit programmable in 25ms steps	0	0 (0000000) 25 (0000001) 50 . . 3175 (1111111)	3175	ms
Time for Flash to Turn On, t_3	7-bit programmable in 25ms steps	0	0 (0000000) 25 (0000001) 50 . . 3175 (1111111)	3175	ms
Time for Flash to Turn On, t_4	7-bit programmable in 25ms steps	0	0 (0000000) 25 (0000001) 50 . . 3175 (1111111)	3175	ms

FLASH TIMER ELECTRICAL CHARACTERISTICS (continued)

(MAX8982A/MAX8982P: $V_{IN1A} = V_{IN1B} = +5V$ and $V_{DD\_} = +3.2V$, MAX8982X: $V_{IN1A} = V_{IN1B} = +3.3V$ and $V_{DD\_} = +3.3V$, $C_{REFBP} = 0.1\mu F$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 4, Figure 11)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Programmable On-Time, t_{ON}	4-bit programmable in 25ms steps, same for each flash timer	25		400	ms
		25 (0000) 50 (0001) 75 . . 400 (1111)			

N32KHZ ELECTRICAL CHARACTERISTICS

(MAX8982A/MAX8982P: $V_{DD\_} = +3.2V$, MAX8982X: $V_{DD\_} = +3.3V$, $V_{BUCK2} = 1.8V$, $C_{BUCK2} = 2.2\mu F$, $C_{REFBP} = 0.1\mu F$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output High Voltage	Internal logic supply I_{SOURCE} = 2mA	V_{BUCK2} - 0.45V			V
Output Low Voltage	Internal logic supply I_{SINK} = 2mA			0.45	V
Output Duty Cycle		30	50	70	%
Output Frequency Range	Including initial startup, 20% tolerance	25.6	32	38.4	kHz
Startup Time	From BUCK2 enable (Figure 4)			225	µs
Edge Jitter (Note 4)				10	ns

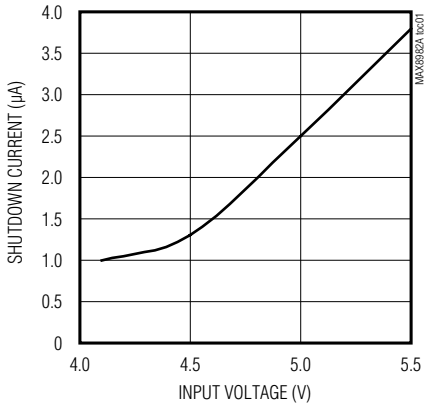
Note 3: Limits are 100% production tested at T_A = +25°C, unless otherwise noted. Limits over the temperature range are guaranteed by design.

Note 4: Guaranteed by design, not production tested.

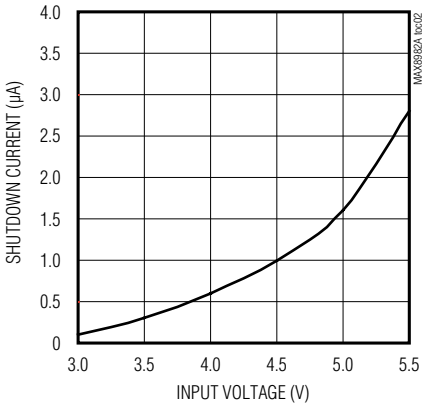
Typical Operating Characteristics

(MAX8982A/MAX8982P: $V_{IN1A} = V_{IN1B} = 5V$, MAX8982X: $V_{IN1A} = V_{IN1B} = V_{DDA} = V_{DDB} = V_{IN4} = 3.3V$, $C_{REFBP} = 0.1\mu F$, T_A = -40°C to +85°C, Circuits of Figures 2 and 3, unless otherwise noted. Typical values are at T_A = +25°C. Limits are 100% production tested at T_A = +25°C, unless otherwise noted. Limits over the temperature range are guaranteed by design.)

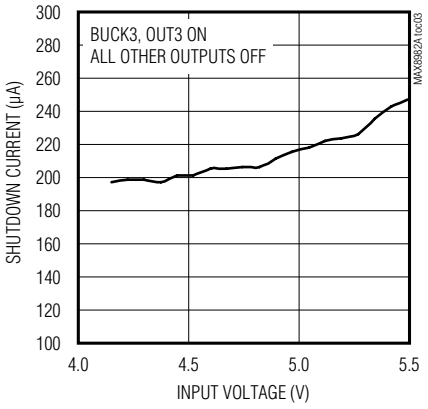
SHUTDOWN CURRENT vs. INPUT VOLTAGE (MAX8982A)



SHUTDOWN CURRENT vs. INPUT VOLTAGE (MAX8982X)



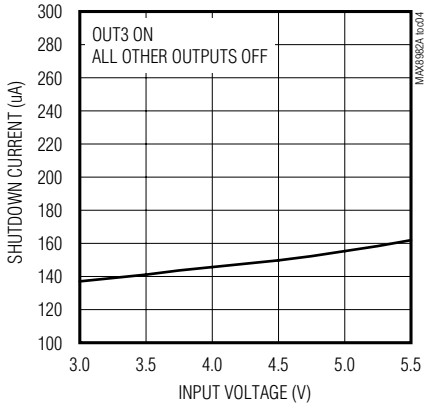
NO LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (MAX8982A)



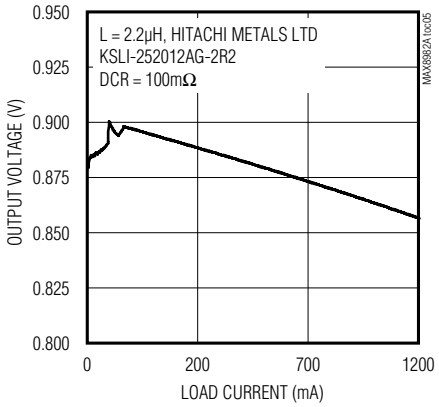
Typical Operating Characteristics (continued)

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = 5V, MAX8982X: V_{IN1A} = V_{IN1B} = V_{DDA} = V_{DDB} = V_{IN4} = 3.3V, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, Circuits of Figures 2 and 3, unless otherwise noted. Typical values are at T_A = +25°C. Limits are 100% production tested at T_A = +25°C, unless otherwise noted. Limits over the temperature range are guaranteed by design.)

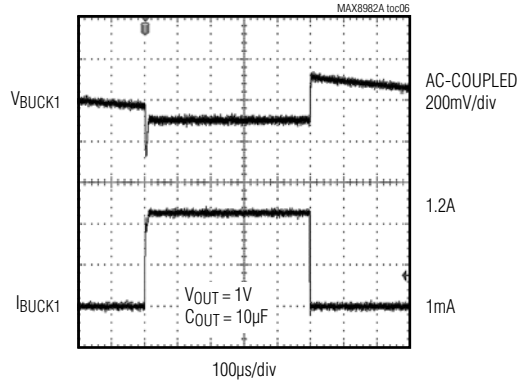
NO LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (MAX8982X)



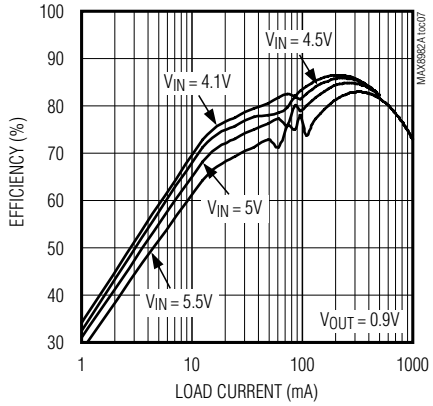
BUCK1 LOAD REGULATION



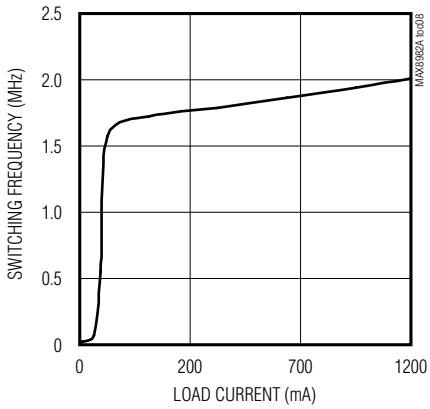
BUCK1 LOAD TRANSIENT



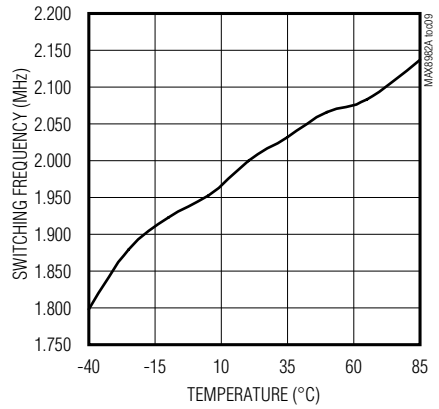
BUCK1 EFFICIENCY vs. LOAD CURRENT



BUCK1 SWITCHING FREQUENCY vs. LOAD CURRENT



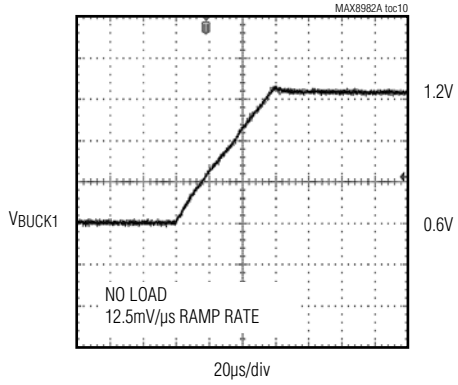
BUCK1 SWITCHING FREQUENCY vs. TEMPERATURE



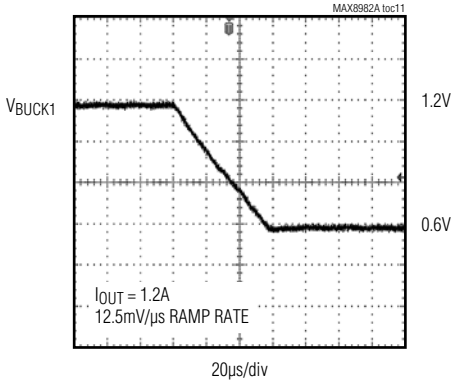
Typical Operating Characteristics (continued)

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = 5V, MAX8982X: V_{IN1A} = V_{IN1B} = V_{DDA} = V_{DDB} = V_{IN4} = 3.3V, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, Circuits of Figures 2 and 3, unless otherwise noted. Typical values are at T_A = +25°C. Limits are 100% production tested at T_A = +25°C, unless otherwise noted. Limits over the temperature range are guaranteed by design.)

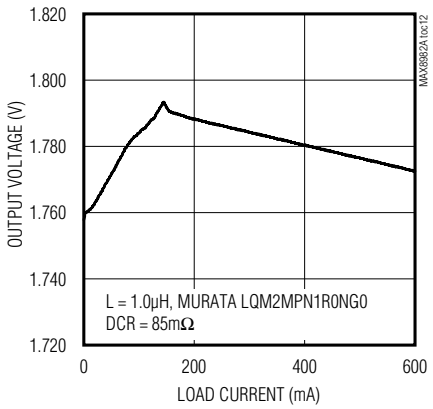
BUCK1 RAMP-UP TRANSITION



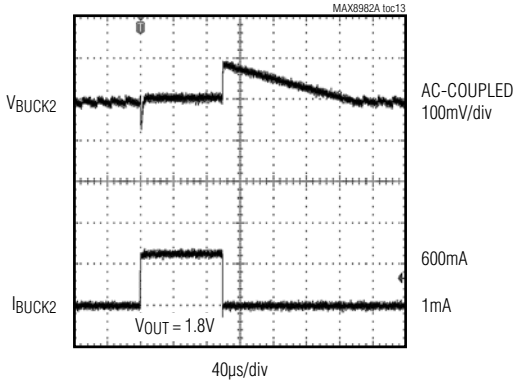
BUCK1 RAMP-DOWN TRANSITION



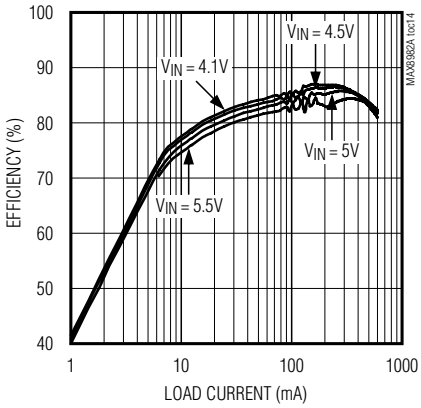
BUCK2 LOAD REGULATION



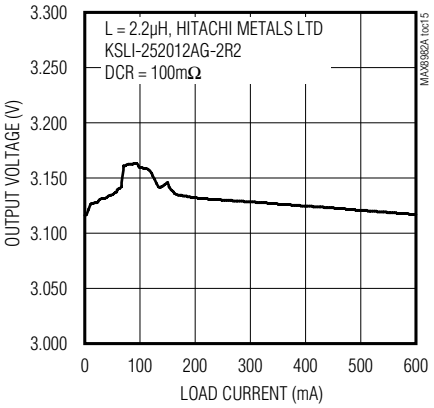
BUCK2 LOAD TRANSIENT



BUCK2 EFFICIENCY vs. LOAD CURRENT



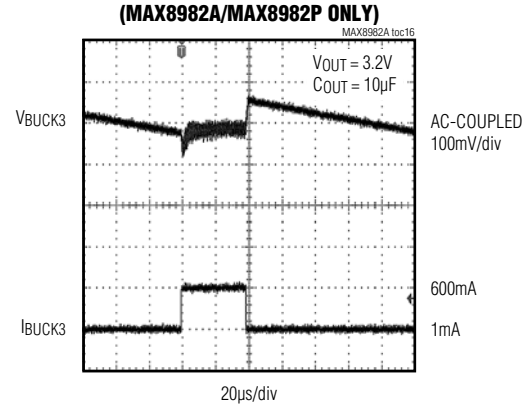
BUCK3 LOAD REGULATION (MAX8982A/MAX8982P ONLY)



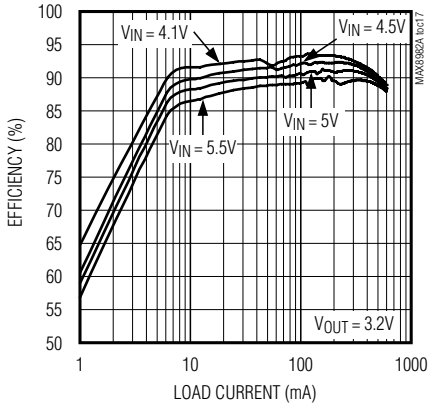
Typical Operating Characteristics (continued)

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = 5V, MAX8982X: V_{IN1A} = V_{IN1B} = V_{DDA} = V_{DDB} = V_{IN4} = 3.3V, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, Circuits of Figures 2 and 3, unless otherwise noted. Typical values are at T_A = +25°C. Limits are 100% production tested at T_A = +25°C, unless otherwise noted. Limits over the temperature range are guaranteed by design.)

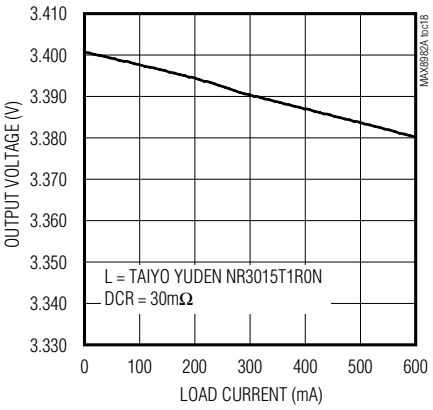
BUCK3 LOAD TRANSIENT (MAX8982A/MAX8982P ONLY)



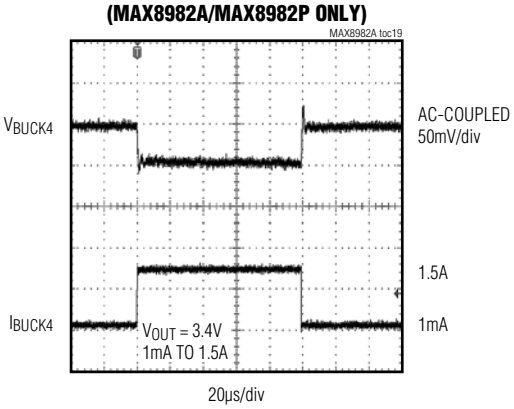
BUCK3 EFFICIENCY vs. LOAD CURRENT (MAX8982A/MAX8982P ONLY)



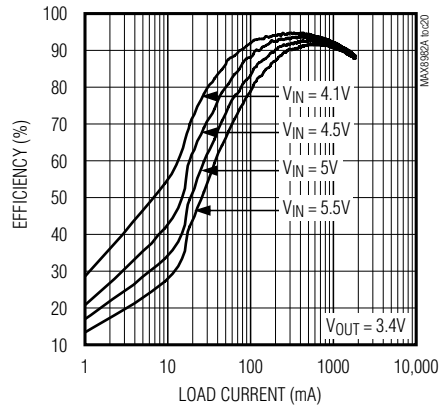
BUCK4 LOAD REGULATION (MAX8982A/MAX8982P ONLY)



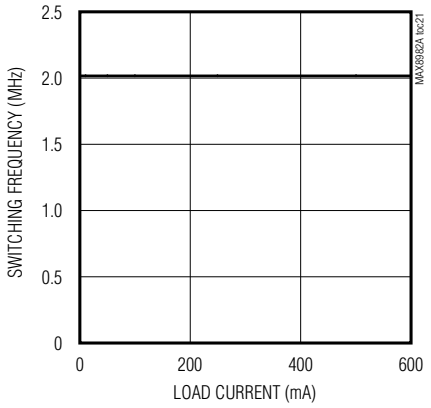
BUCK4 LOAD TRANSIENT (MAX8982A/MAX8982P ONLY)



BUCK4 EFFICIENCY vs. LOAD CURRENT (MAX8982A/MAX8982P ONLY)



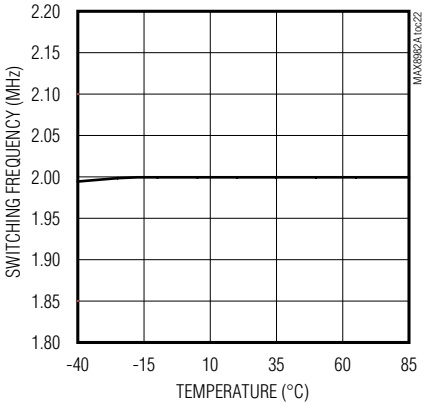
BUCK4 SWITCHING FREQUENCY vs. LOAD CURRENT (MAX8982A/MAX8982P ONLY)



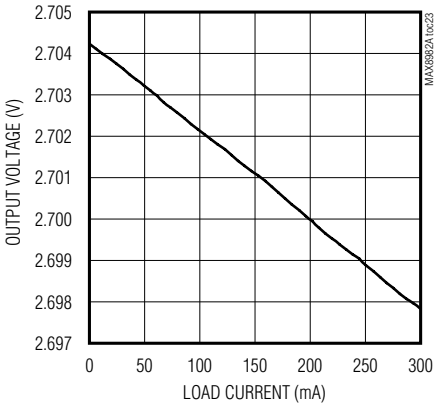
Typical Operating Characteristics (continued)

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = 5V, MAX8982X: V_{IN1A} = V_{IN1B} = V_{DDA} = V_{DDB} = V_{IN4} = 3.3V, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, Circuits of Figures 2 and 3, unless otherwise noted. Typical values are at T_A = +25°C. Limits are 100% production tested at T_A = +25°C, unless otherwise noted. Limits over the temperature range are guaranteed by design.)

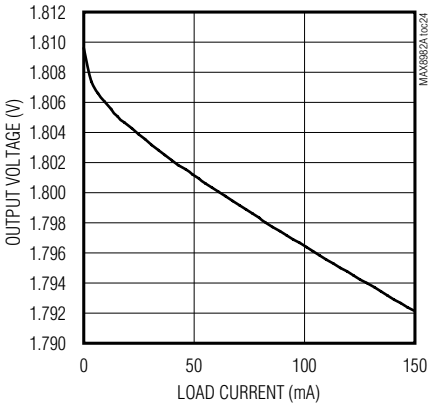
BUCK4 SWITCHING FREQUENCY vs. TEMPERATURE (MAX8982A/MAX8982P ONLY)



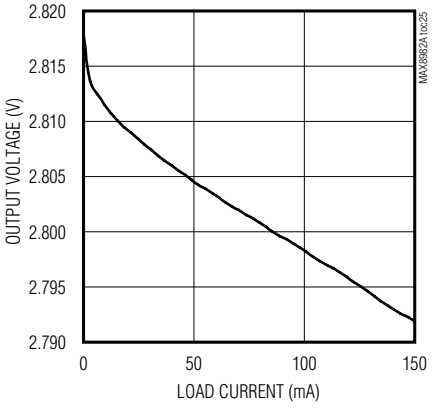
LDO1 LOAD REGULATION



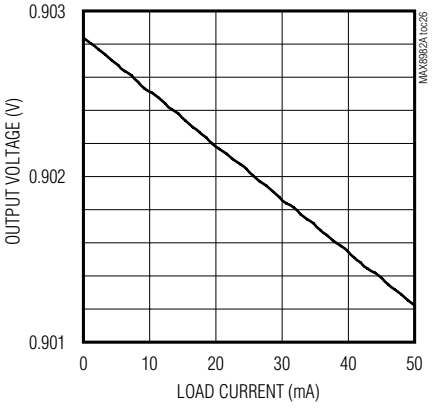
LDO2 LOAD REGULATION



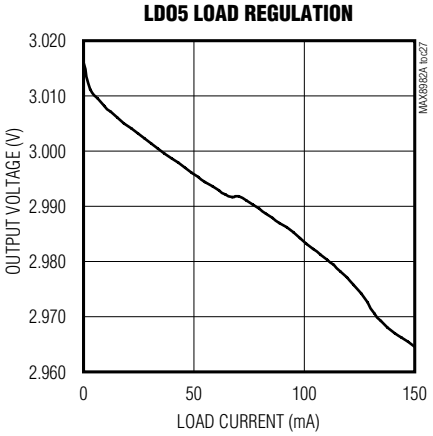
LDO3 LOAD REGULATION



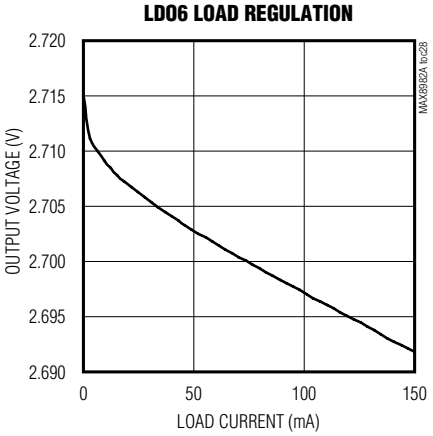
LDO4 LOAD REGULATION



LDO5 LOAD REGULATION



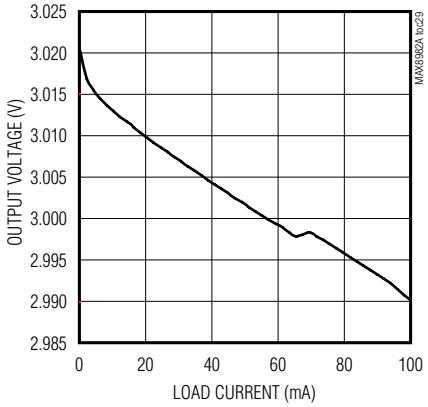
LDO6 LOAD REGULATION



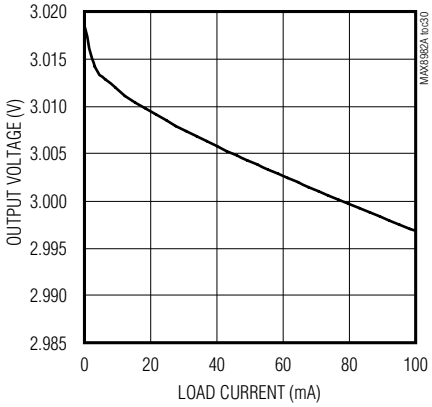
Typical Operating Characteristics (continued)

(MAX8982A/MAX8982P: V_{IN1A} = V_{IN1B} = 5V, MAX8982X: V_{IN1A} = V_{IN1B} = V_{DDA} = V_{DDB} = V_{IN4} = 3.3V, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, Circuits of Figures 2 and 3, unless otherwise noted. Typical values are at T_A = +25°C. Limits are 100% production tested at T_A = +25°C, unless otherwise noted. Limits over the temperature range are guaranteed by design.)

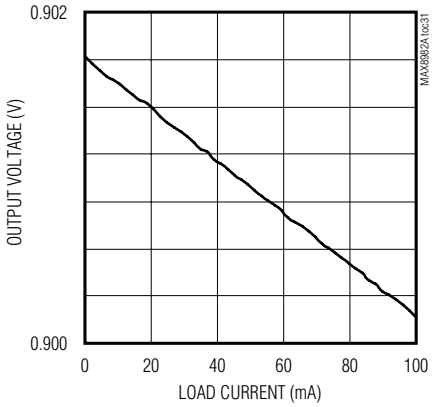
LDO7 LOAD REGULATION



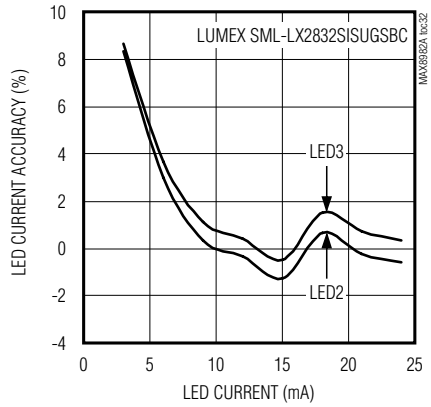
LDO8 LOAD REGULATION (MAX8982A/MAX8982P ONLY)



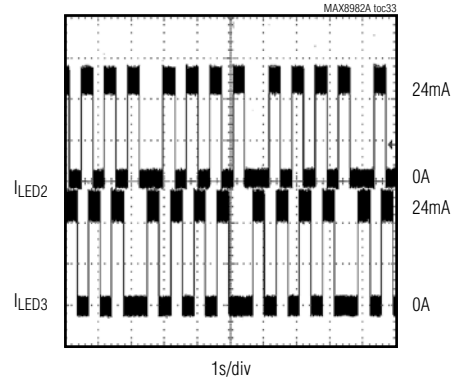
LDO9 LOAD REGULATION



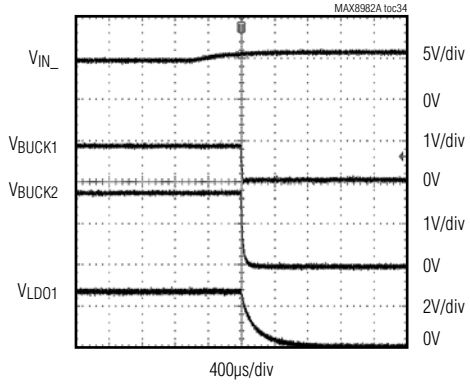
LED CURRENT ACCURACY vs. LED CURRENT SETTING



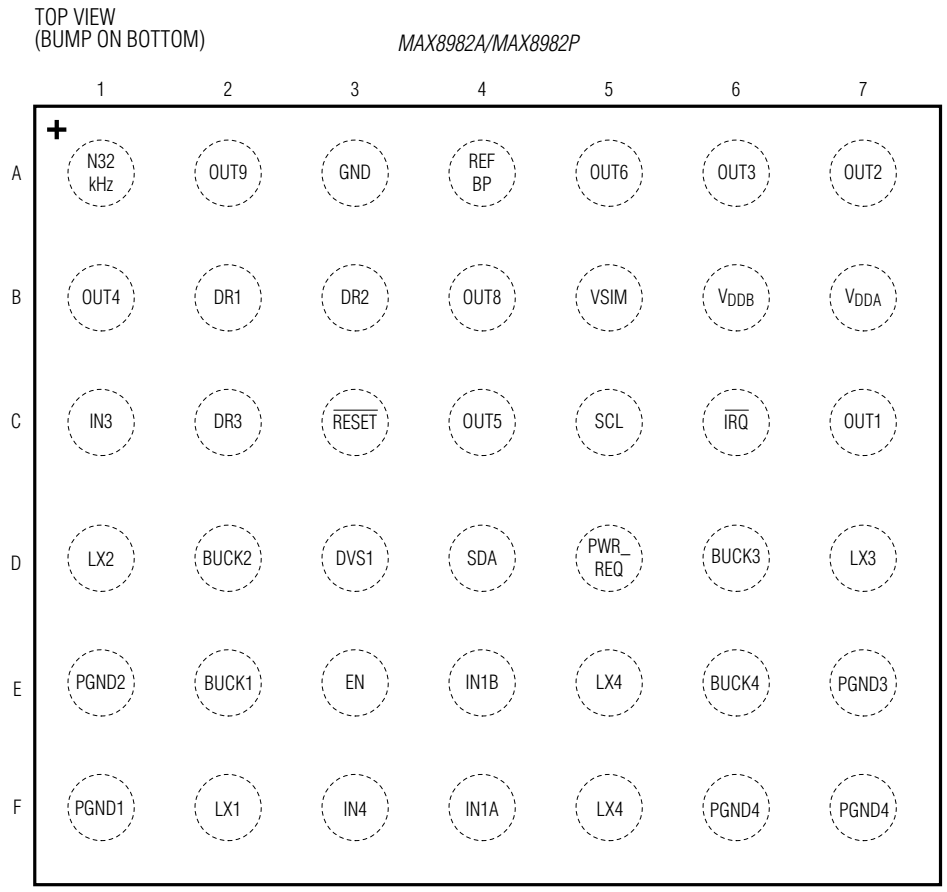
LED FLASH WAVEFORMS



OVERVOLTAGE PROTECTION

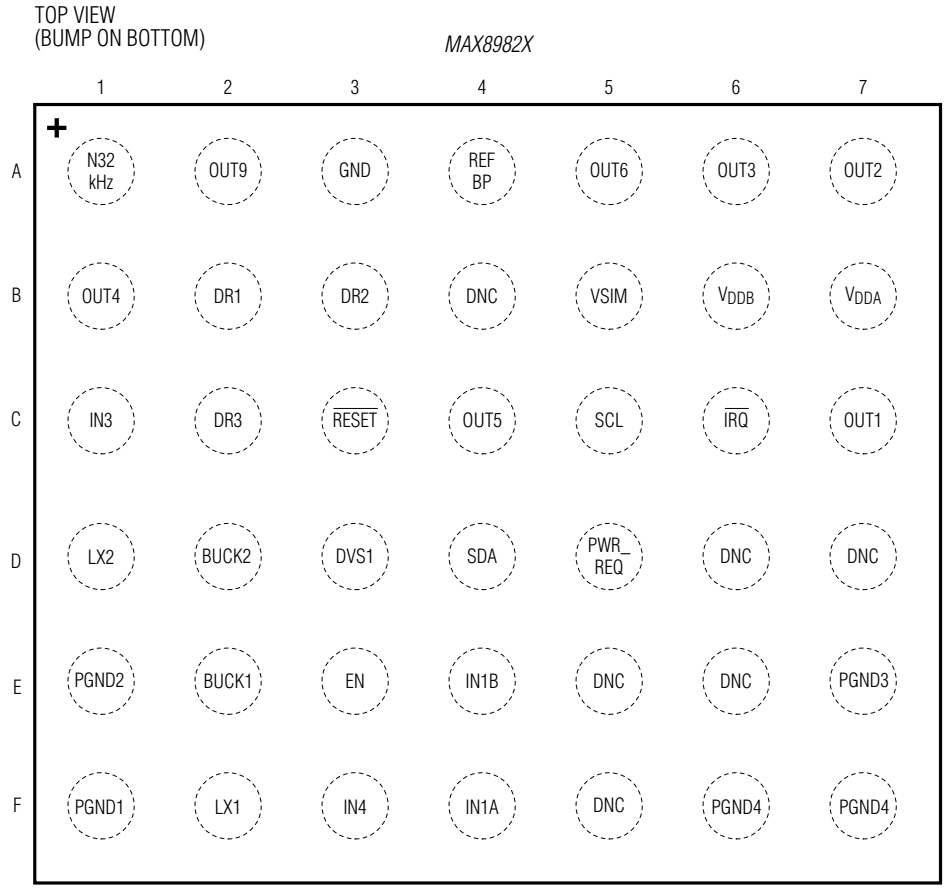


Pin Configurations



WLP

Pin Configurations (continued)



WLP

Pin Description

PIN	NAME		FUNCTION
	MAX8982A/ MAX8982P	MAX8982X	
GROUND			
A3	GND	GND	Analog Ground
F1	PGND1	PGND1	Power Ground for BUCK1
E1	PGND2	PGND2	Power Ground for BUCK2
E7	PGND3	PGND3	Power Ground for BUCK3
F6, F7	PGND4	PGND4	Power Ground for BUCK4
INPUT SUPPLY			
F4	IN1A	—	Input Supply to the IC. The operating voltage range for the MAX8982A is 4.1V to 5.5V. Connect three 330µF tantalum capacitors as close as possible to IN1A and IN1B. Connect IN1A to IN1B.
	—	IN1A	Input Supply to the IC. The operating voltage range for the MAX8982X is 2.9V to 5.5V. Bypass with a 22µF ceramic capacitor as close as possible to IN1A and IN1B. Connect IN1A to IN1B.
E4	IN1B	IN1B	Input Supply to the IC. Connect IN1B to IN1A.
C1	IN3	IN3	Input Supply for LDO4 and LDO9. Connect IN3 to the BUCK2 output. Bypass IN3 with a 2.2µF ceramic capacitor as close as possible to IN3.
F3	IN4	—	Input Supply for LDO8. Bypass with a 1µF ceramic capacitor as close as possible to IN4. The IN4 operating range is from 3.0V to 5.5V. Connect IN4 to either IN1A and IN1B.
	—	IN4	Connect IN4 to Both IN1A and IN1B
B7	V_{DDA}	—	Power Input for LDO1 and LDO2. Connect V_{DDA} to V_{DDB}. Bypass V_{DDA} with a 10µF ceramic capacitor as close as possible to V_{DDA}.
	—	V_{DDA}	Power Input for LDO1 and LDO2. Connect V_{DDA} to V_{DDB}, IN1A, and IN1B.
B6	V_{DDB}	—	Power Input for LDO3, LDO5, LDO6, and LDO7. Connect V_{DDB} to V_{DDA}.
	—	V_{DDB}	Power Input for LDO3, LDO5, LDO6, and LDO7. Connect V_{DDB} to V_{DDA}, IN1A, and IN1B.
BUCK CONVERTERS			
F2	LX1	LX1	BUCK1 Inductor Connection. LX1 connects to the drains of the internal p-channel and n-channel MOSFETs.
D1	LX2	LX2	BUCK2 Inductor Connection. LX2 connects to the drains of the internal p-channel and n-channel MOSFETs.
D7	LX3	—	BUCK3 Inductor Connection. LX3 connects to the drains of the internal p-channel and n-channel MOSFETs.
	—	DNC	Do Not Connect
E5, F5	LX4	—	BUCK4 Inductor Connection. LX4 connects to the drains of the internal p-channel and n-channel MOSFETs. Connect the two LX4 bumps together externally.
	—	DNC	Do Not Connect
E2	BUCK1	BUCK1	BUCK1 Output Feedback
D2	BUCK2	BUCK2	BUCK2 Output Feedback
D6	BUCK3	—	BUCK3 Output Feedback
	—	DNC	Do Not Connect
E6	BUCK4	—	BUCK4 Output Feedback
	—	DNC	Do Not Connect

Pin Description (continued)

PIN	NAME		FUNCTION
	MAX8982A/ MAX8982P	MAX8982X	
LDO REGULATORS			
C7	OUT1	OUT1	LDO1 Output. Bypass OUT1 with a 4.7µF ceramic capacitor. OUT1 supplies loads up to 300mA. The default output voltage is 2.7V.
A7	OUT2	OUT2	LDO2 Output. Bypass OUT2 with a 1µF ceramic capacitor. OUT2 supplies loads up to 150mA. The default output voltage is 1.8V.
A6	OUT3	OUT3	LDO3 Output. Bypass OUT3 with a 1µF ceramic capacitor. OUT3 supplies loads up to 150mA. The default output voltage is 2.8V.
B1	OUT4	OUT4	LDO4 Output. Bypass OUT4 with a 2.2µF ceramic capacitor. OUT4 supplies loads up to 50mA. The default output voltage is 0.9V.
C4	OUT5	OUT5	LDO5 Output. Bypass OUT5 with a 1µF ceramic capacitor. OUT5 supplies loads up to 150mA. The default output voltage is 3.0V.
A5	OUT6	OUT6	LDO6 Output. Bypass OUT6 with a 1µF ceramic capacitor. OUT6 supplies loads up to 150mA. The default output voltage is 2.7V.
B5	VSIM	VSIM	LDO7 Output. Bypass VSIM with a 1µF ceramic capacitor. VSIM supplies loads up to 150mA. The default output voltage is 3V.
B4	OUT8	—	LDO8 Output. Bypass OUT8 with a 1µF ceramic capacitor. OUT8 supplies loads up to 150mA. The default output voltage is 3V.
	—	DNC	Do Not Connect
A2	OUT9	OUT9	LDO9 Output. Bypass OUT9 with a 2.2µF ceramic capacitor. OUT9 supplies loads up to 50mA. The default output voltage is 0.9V.
I²C INTERFACE			
D4	SDA	SDA	I²C Data. SDA is high impedance when off.
C5	SCL	SCL	I²C Clock. SCL is high impedance when off.
CURRENT REGULATORS			
B2	DR1	DR1	Current Regulated Driver 1. Typically used to drive an LED. DR1 can be programmed to sink 3mA to 24mA in 8 steps (24mA default). If the flash timer is activated, the LED can be programmed to turn on/off in a preprogrammed pattern. See the *Embedded Flash Timer* section.
B3	DR2	DR2	Current Regulated Driver 2. Typically used to drive an LED. DR2 can be programmed to sink 3mA to 24mA in 8 steps (24mA default). If the flash timer is activated, the LED can be programmed to turn on/off in a preprogrammed pattern. See the *Embedded Flash Timer* section.
C2	DR3	DR3	Current Regulated Driver 3. Typically used to drive an LED. DR3 can be programmed to sink 3mA to 24mA in 8 steps (24mA default). If the flash timer is activated, the LED can be programmed to turn on/off in a preprogrammed pattern. See the *Embedded Flash Timer* section.
LOGIC INPUTS			
E3	EN	EN	Active-High IC Enable Input
D5	PWR_REQ	PWR_REQ	Active-High to Enable All Designated Step-Down Regulators and LDOs in Sequence. Active-high/low to enable/disable all step-down converters and LDOs after power-on. The values in the BUCK1DVS1 and BUCK1DVS2 registers are reset to their defaults when PWR_REQ goes low in normal operation.
D3	DVS1	DVS1	BUCK1 Output Selection Input for DVS Function

Pin Description (continued)

PIN	NAME		FUNCTION
	MAX8982A/ MAX8982P	MAX8982X	
LOGIC OUTPUTS			
C6	$\overline{IRQ}$	$\overline{IRQ}$	Active-Low, Open-Drain Interrupt Output. Internal pullup resistor, 200kΩ, to BUCK2.
C3	$\overline{RESET}$	$\overline{RESET}$	Active-Low, Open-Drain Reset Output. There is an internal 14kΩ pullup resistor to BUCK2.
REFERENCE OUTPUT			
A4	REFBP	REFBP	Reference Bypass. Connect the reference bypass capacitor from REFBP to GND. See Table 3. High impedance in off condition. V_{REFBP} is 0.8V (typ). Do not use to provide power to external circuitry.
32kHz CLOCK			
A1	N32kHz	N32kHz	32kHz Clock Output. This output is supplied from BUCK2.

Table 1. Summary of Power Supplies

PARAMETER	BUCK1	BUCK2	BUCK3*	BUCK4*	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7 (VSIM)	OUT8*	OUT9
Function	Core	System IO	LDO INPUT	PA	RF	RF	Analog	PLL	SD	TCXO	SIM	USB	BB
Default Voltage (V)	**0.9**	**1.8**	**3.2**	**3.4**	**2.7**	**1.8**	**2.8**	**0.9**	**3.0**	**2.7**	**3.00**	**3.0**	**0.9**
Continuous Output Current (mA)	1200** 1300***	600	600	1800	300	150	150	50	150	150	150	150	50
Programmable Voltage Options (V)	0.600	N/A	2.90	3.00	2.65	1.5	2.65	0.8	2.80	2.65	1.80	3.00	0.8
	25mV step		2.95	3.05	2.70	1.8	2.70	0.9	2.90	2.70	3.00	3.10	0.9
			3.00	3.10	2.75	2.7	2.75	1.0	3.00	2.75		3.20	1.0
			3.05	3.15	2.80	1.7	2.80	1.1	3.20	2.80		3.30	1.1
			3.10	3.20	2.85		2.85	1.2		2.85			1.2
			3.15	3.25	2.90		2.90			2.90			
			3.20	3.30	2.95		2.95			2.95			
			3.25	3.35	3.00		3.00			3.00			
			3.30	3.40									
			3.35	3.45									
			3.40	3.50									
			3.45	3.55									
			3.50	3.60									
			3.55	3.65									
			3.60	3.70									
	1.20		3.65	3.75									

**BUCK3, BUCK4, and OUT8 are for the MAX8982A/MAX8982P only.*
***MAX8982A/MAX8982X.*
****MAX8982P.*

Table 1. Summary of Power Supplies (continued)

PARAMETER	BUCK1	BUCK2	BUCK3*	BUCK4*	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	OUT7 (VSIM)	OUT8*	OUT9
Default ON at Initial Startup	PWR_ REQ	**ON**	**ON**	OFF	PWR_ REQ	PWR_ REQ	**ON**	PWR_ REQ	OFF	PWR_ REQ	OFF	**ON**	ON
ON/OFF Control After Power-Up	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ	I²C or PWR_ REQ
Default Active Discharge Resistor	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

**BUCK3, BUCK4, and OUT8 are for the MAX8982A/MAX8982P only.*

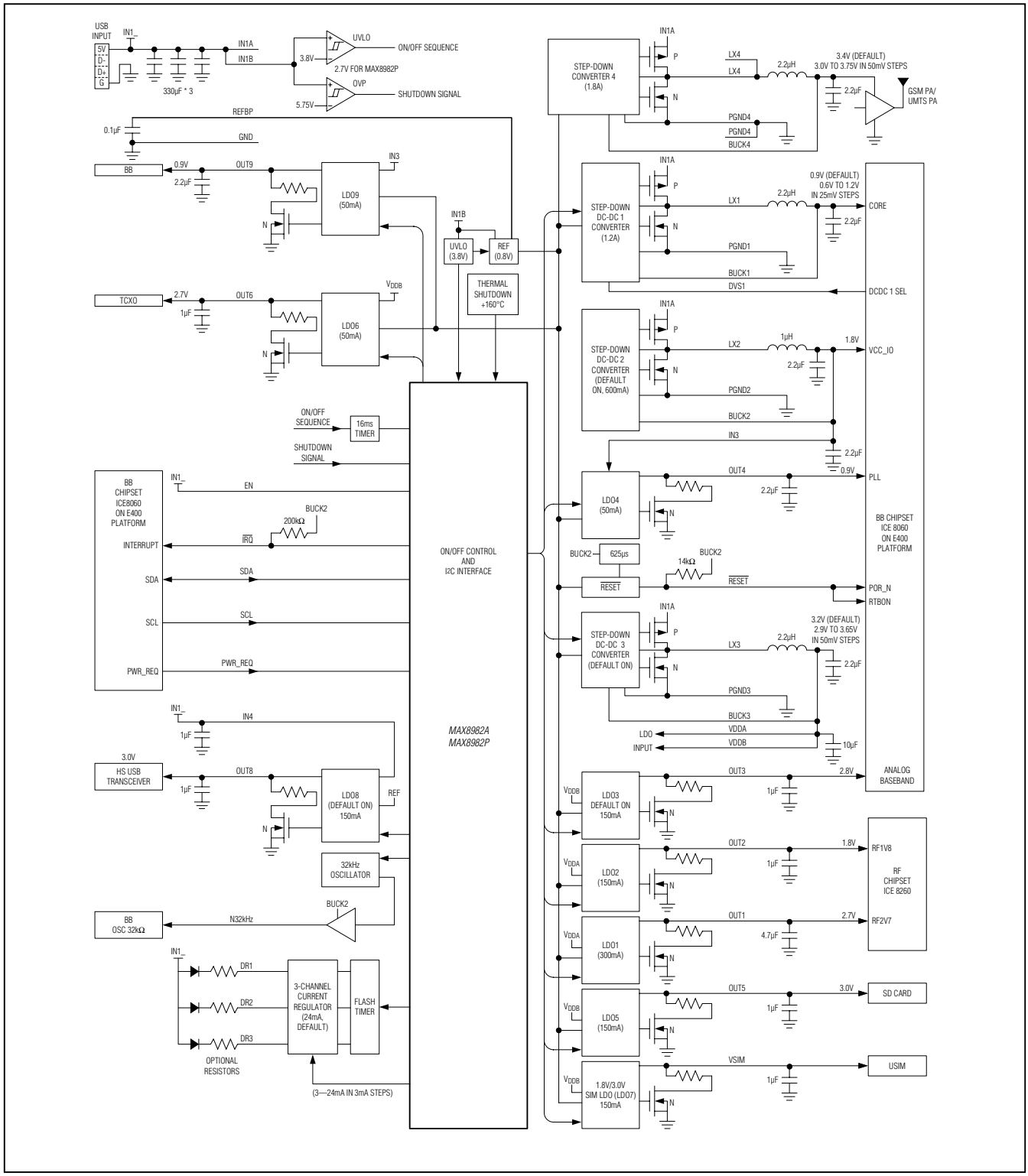


Figure 1. MAX8982A/MAX8982P Typical Application Circuit and Functional Block Diagram

Table 2. External Component List for Figure 1

LOCATION	EXTERNAL COMPONENTS	NOTES
IN1A, IN1B	3 x 330µF tantalum capacitors	Buck stability and GSM PA supply
IN3	2.2µF	Input for LDO4 and LDO9
IN4	1.0µF	Input for LDO8
OUT1	4.7µF	LDO compensation and load transient response
OUT2	1.0µF	LDO compensation
OUT3	1.0µF	LDO compensation
OUT4	2.2µF	LDO compensation
OUT5	1.0µF	LDO compensation
OUT6	1.0µF	LDO compensation
VSIM (OUT7)	1.0µF	LDO compensation
OUT8	1.0µF	LDO compensation
OUT9	2.2µF	LDO compensation
V_{DDA}, V_{DDB}	Total capacitance ≥ total output capacitance for LDO1, LDO2, LDO3, LDO5, LDO6, and VSIM. Use a 10µF capacitor on V_{DDA}/V_{DDB} as recommended.	All LDOs stability
BUCK1 for BB Core	2.2µF	For low noise, 1.2A continuous load
BUCK2 for BB System IO	2.2µF	For low noise
BUCK3 as LDO Input	2.2µF	For low noise
BUCK4 for GSM PA/UMTS PA	2 x 22µF	Supply for both GSM PA and UMTS PA
LX1	1µH to 4.7µH	2.2µH recommended (Table 60)
LX2	1µH to 4.7µH	1.0µH recommended (Table 60)
LX3	1µH to 4.7µH	2.2µH recommended (Table 60)
LX4	1µH to 4.7µH	2.2µH recommended (Table 60)
REFBP	0.1µF	Noise filter
EN	A pulldown resistor, if necessary.	
Any Bump Required to Pass 8kV Module Level ESD	0.1µF	Absorb ESD energy

Note: *Input/output capacitance should be as close as possible to the IC. All capacitors are ceramic X5R or X7R, unless otherwise noted.*

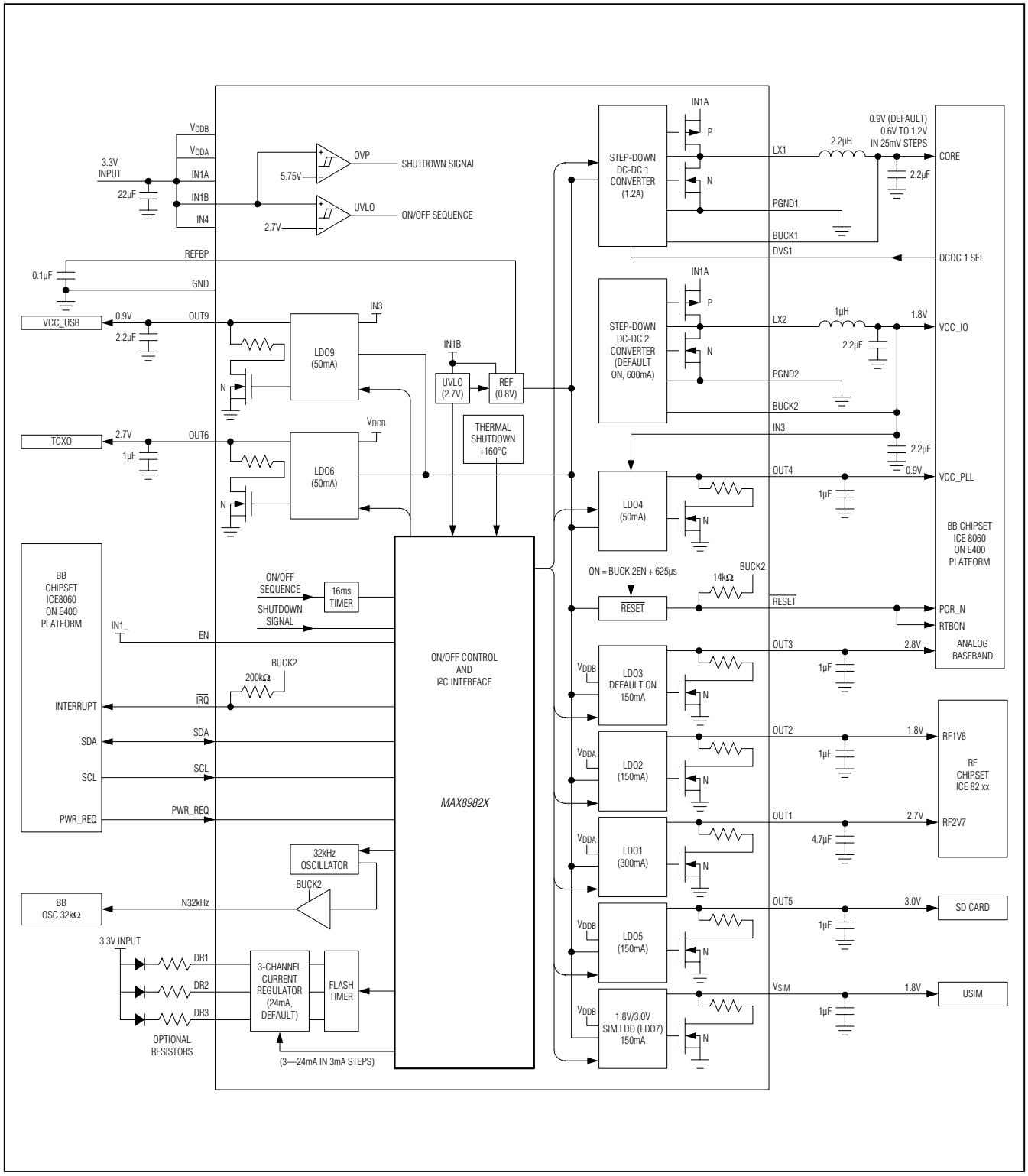


Figure 2. MAX8982X Typical Application Circuit and Functional Block Diagram

Table 3. External Component List for Figure 2

LOCATION	EXTERNAL COMPONENTS	NOTES
IN1A, IN1B	22µF	Buck stability
IN3	2.2µF	Input for LDO4 and LDO9
IN4		Connect to IN1A and IN1B
OUT1	4.7µF	LDO compensation and load transient response
OUT2	1.0µF	LDO compensation
OUT3	1.0µF	LDO compensation
OUT4	2.2µF	LDO compensation
OUT5	1.0µF	LDO compensation
OUT6	1.0µF	LDO compensation
VSIM (OUT7)	1.0µF	LDO compensation
OUT9	2.2µF	LDO compensation
V_{DDA}, V_{DDB}	Total capacitance ≥ total output capacitance for LDO1, LDO2, LDO3, LDO5, LDO6, and VSIM.	All LDOs stability. Connect V_{DDA} and V_{DDB} to IN1A and IN1B.
BUCK1 for BB Core	2.2µF	For low noise, 1.2A continuous load
BUCK2 for BB System IO	2.2µF	For low noise
LX1	1µH to 4.7µH	2.2µH recommended (Table 60)
LX2	1µH to 4.7µH	1.0µH recommended (Table 60)
REFBP	0.1µF	Noise filter
EN	A pulldown resistor, if necessary	
Any Bump Required to Pass 8kV Module Level ESD	0.1µF	Absorb ESD energy

Note: *Input/output capacitance should be as close as possible to the IC. All capacitors are ceramic X5R or X7R, unless otherwise noted.*

Detailed Description

Power-On/Off Control

The power-on/off state diagram is shown in Figure 3. When the IN1_ supply voltage is valid and EN is high, the default power supplies turn on in sequence (Figure 4). Once powered up, any step-down or LDO output can be enabled or disabled through I²C, or they can be programmed to be controlled by the PWR_REQ logic input.

PWR_REQ

PWR_REQ is a control input from baseband chipset used to enable/disable specified regulators.

After power-up, when PWR_REQ goes logic-high, any step-down or LDO output programmed for PWR_REQ control is enabled in a predefined sequence. The regulators are powered up in four groups as shown in Figure 5. See the following for the regulators belonging to each group. When PWR_REQ goes logic-low, all regulators programmed for PWR_REQ control are turned off simultaneously.

Any regulator that is set to on or off though I²C is not affected by PWR_REQ, except for BUCK1. The programmed values in BUCK1DVS1 and BUCK1DVS2 are reset to their defaults when PWR_REQ goes low even in normal operation.

Group A: BUCK3 (MAX8982A/MAX8982P only)
LDO2 (default is PWR_REQ On mode)
BUCK2

Group B: LDO1 (default is PWR_REQ On mode)
LDO3
BUCK4 (MAX8982A/MAX8982P only)

Group C: LDO6 (default is PWR_REQ On mode)
LDO5
LDO7
LDO8 (MAX8982A/MAX8982P only)

Group D: BUCK1 (default is PWR_REQ On mode)
LDO4 (default is PWR_REQ On mode)
LDO9

Active Discharge

All regulators include an internal resistor for discharging the output when the regulator is shut down. In the default state (except BUCK2), this resistor is not connected so the output decay depends only on the applied load. To enable this discharge resistor, set the appropriate bit in the BUCK1-4ADIS, LDO1-8ADIS, or LDO9ADIS register. The active discharge resistor values are specified in the *General Electrical Characteristics* table.

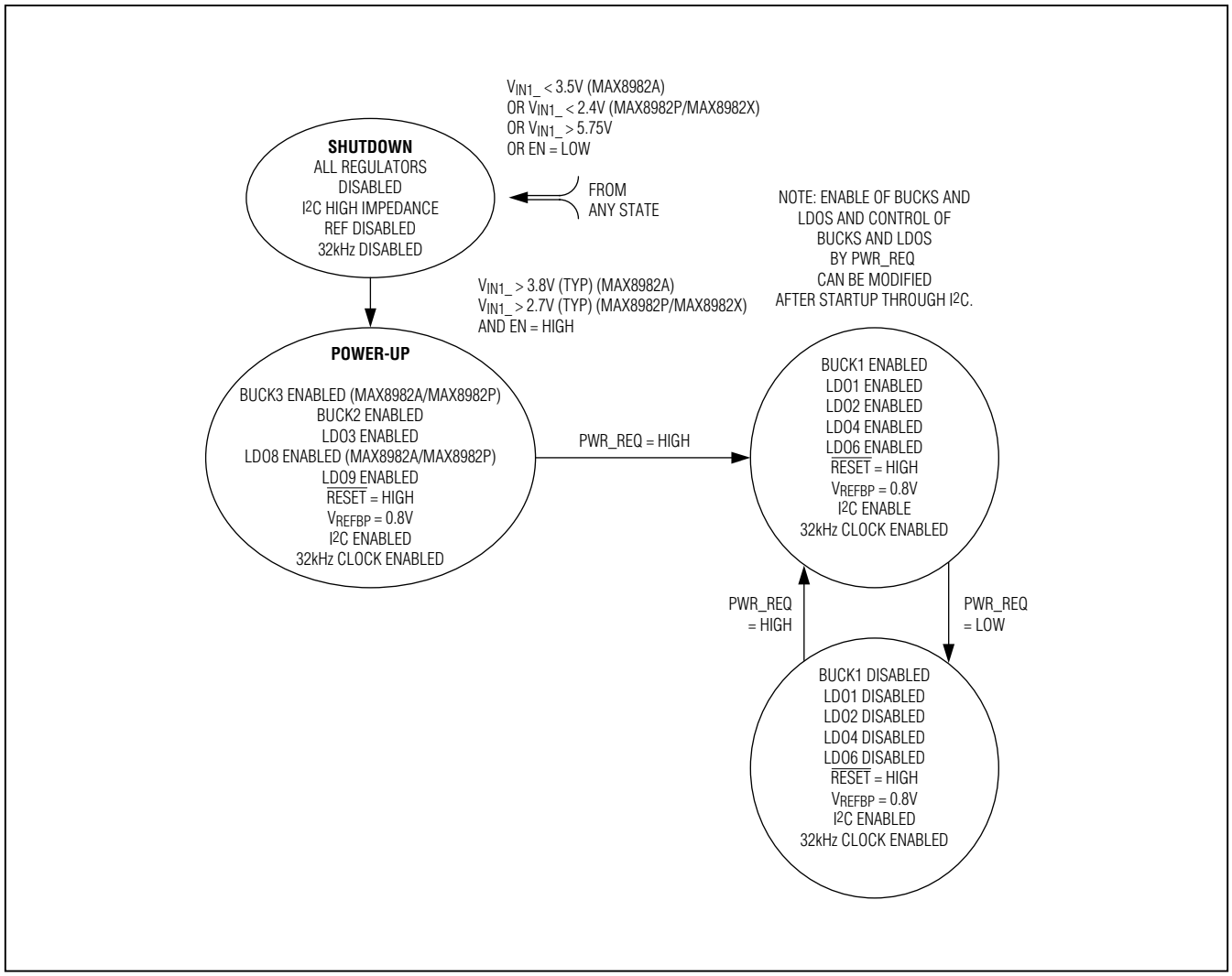


Figure 3. Power-On/Off State Diagram with IN3 Connected to BUCK2 Output and IN4 Connected to IN1_. Default PWR_REQ Regulators Are Shown.

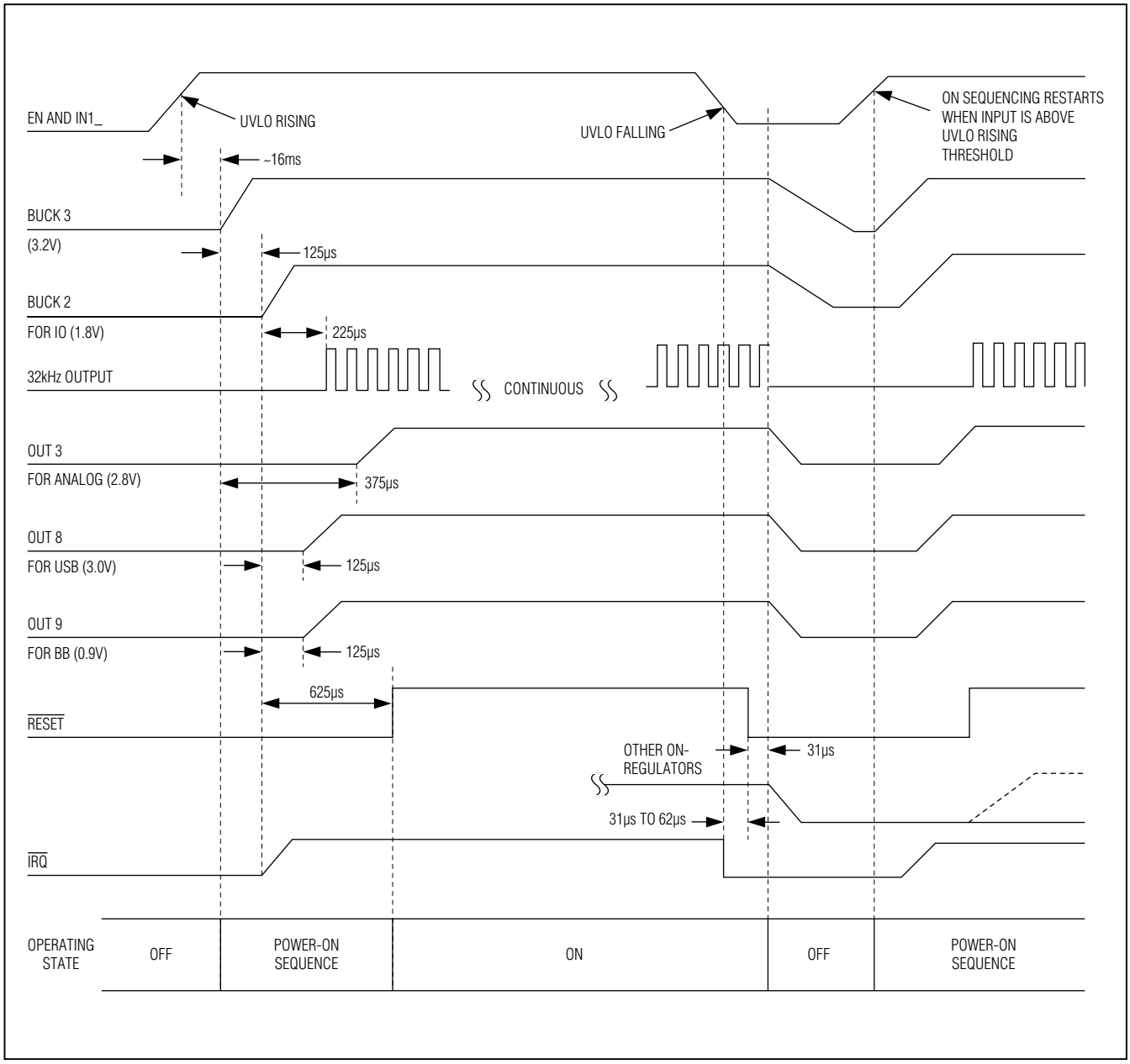


Figure 4. MAX8982_ Power-On Timing Diagram at Initial Startup with EN Connected to IN1_. BUCK3 and OUT8 Are for the MAX8982A/MAX8982P Only.

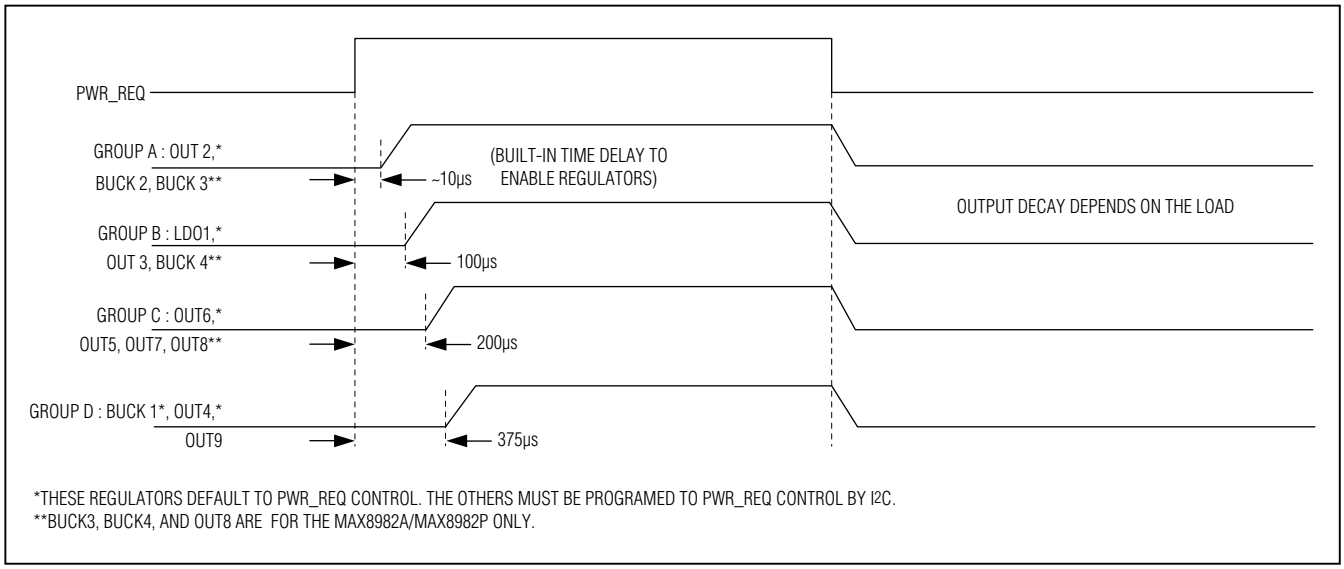


Figure 5. MAX8982_ Power-On Timing Diagram in PWR_REQ ON Mode After Power-Up

BUCK1, BUCK2, and BUCK3 Step-Down Converters

The step-down converters are optimized for high efficiency over a wide load range, small external component size, low output ripple, and excellent transient response. The step-down converters also feature an internal MOSFET switch with optimized on-resistance and an internal synchronous rectifier to maximize the efficiency and reduce the number of external components. The ICs use a proprietary hysteretic PWM control scheme that switches with a nearly fixed frequency. Figure 6 shows the frequency variation versus load current with a 5V input supply and at T_A = +25°C.

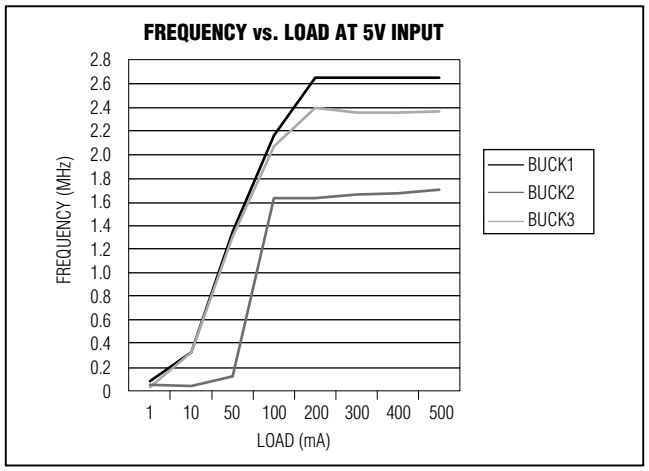


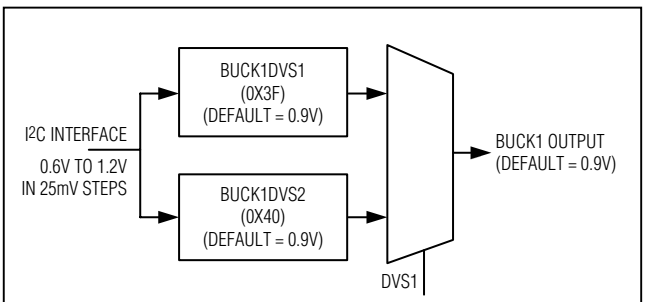
Figure 6. Frequency Variation vs. Load Current with a 5V Input Supply

Setting the Output Voltage on BUCK1

The default output is 0.9V. The BUCK1 voltage is programmable through I²C from 0.6V to 1.2V in 25mV increments.

Dynamic Voltage Scaling (DVS) Function on Buck 1

BUCK1 includes DVS that allows two output voltages to be programmed through I²C, and an external control input to select between the two voltages. Toggling DVS1 changes the BUCK1 output voltage on-the-fly between the two programmed voltages (Figure 7). Each BUCK1DVS_ register specifies a voltage in the 0.6V to 1.2V range in 25mV increments.



Truth Table

DVS1	BUCK1 OUTPUT
High	Set by BUCK1DVS2 register
Low	Set by BUCK1DVS1 register

Figure 7. DVS1 Logic Diagram

Ramp-Up/Down Slope Control on BUCK1

BUCK1 uses a controlled ramp rate when it is enabled and when changing between output voltage settings. Four programmable slew rates are available for BUCK1. The default value is 12.5mV/µs (Table 4). The same slew rate is applied for ramp-up/down.

Setting the Output Voltage on BUCK2

The BUCK2 output voltage is fixed at 1.8V. No programmable output is available.

Setting the Output Voltage on BUCK3

The BUCK3 default output is 3.2V. The BUCK3 output voltage is programmable from 2.9V to 3.65V in 50mV increments through I²C. BUCK3 is only available on the MAX8982A/MAX8982P.

BUCK4 Step-Down Converter for PA (Power Amplifier)

BUCK4 is a 2MHz fixed-frequency PWM step-down converter, typically used to supply the power amplifier (PA). The BUCK4 load capability is 1.8A. BUCK4 is only available on the MAX8982A/MAX8982P.

Setting the Output Voltage on BUCK4

The default output voltage is 3.4V. The BUCK4 output voltage is programmable between 3.0V and 3.75V in 50mV increments through I²C.

Linear Regulators

All linear regulators are designed for low-drop, low noise, high PSRR, and low quiescent current to minimize power consumption. If the input voltage is above UVLO threshold and power-on is logic-high, the default linear regulator (LDO3) turns on. The other LDOs are turned on and off by the baseband processor through the I²C interface or PWR_REQ control signal. All LDO output voltages are programmable through the I²C interface within option voltages.

Table 4. BUCK1 Ramp-Up/Down Slope Control Settings

RASD1[1]	RASD1[0]	SLEW RATE (mV/µs)
0	0	5
0	1	10
1	**0**	**12.5 (default)**
1	1	25

Reference Bypass (REFBP)

The reference bypass is for low noise filtering only and must not be loaded. Bypass REFBP with a 0.1µF ceramic capacitor. The REFBP voltage is 0.8V (typ). Do not use REFBP to provide power to external circuitry.

Thermal Overload Protection

If the internal die temperature of any LDOs or step-down regulators reaches +160°C, the ICs shut down the regulator locally. The regulator is reenabled after it cools by 10°C. The ICs also contain a single +125°C thermal detector located in the center of the die. When the temperature at the center of the die exceeds +125°C, this detector triggers and activates an interrupt.

Undervoltage Lockout (UVLO)

The ICs monitor the voltage at the IN1_ power input. When this voltage drops below 3.5V (MAX8982A) or 2.4V (MAX8982P/MAX8982X), the ICs shut down. The ICs turn on when this voltage rises above 3.8V (MAX8982A) or 2.7V (MAX8982P/MAX8982X) and EN is high. After a UVLO event, all registers are reset to their POR value.

Overvoltage Protection (OVP)

If the voltage on the IN1_ or IN4 inputs exceeds 5.75V (typ), the ICs shut down. When the supply voltage returns to within the valid operating range and EN is high, the ICs turn on and go through a normal power-up sequence. All registers are reset to their default power-on reset (POR) value.

Power-On Reset (POR)

Power-on reset (POR) for I²C occurs when the ICs turn off due to UVLO, OVP, or EN = low. This condition puts the IC into shutdown and then clears all previously programmed output voltages in the internal registers.

The programmed values in BUCK1DVS1 and BUCK1DVS2 are also reset to their defaults when PWR_REQ goes low in normal operation mode.

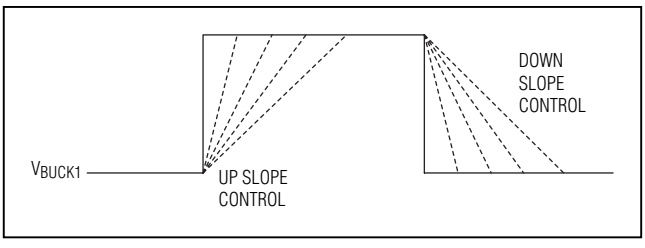


Figure 8. BUCK1 Ramp-Up/Down Slope Control

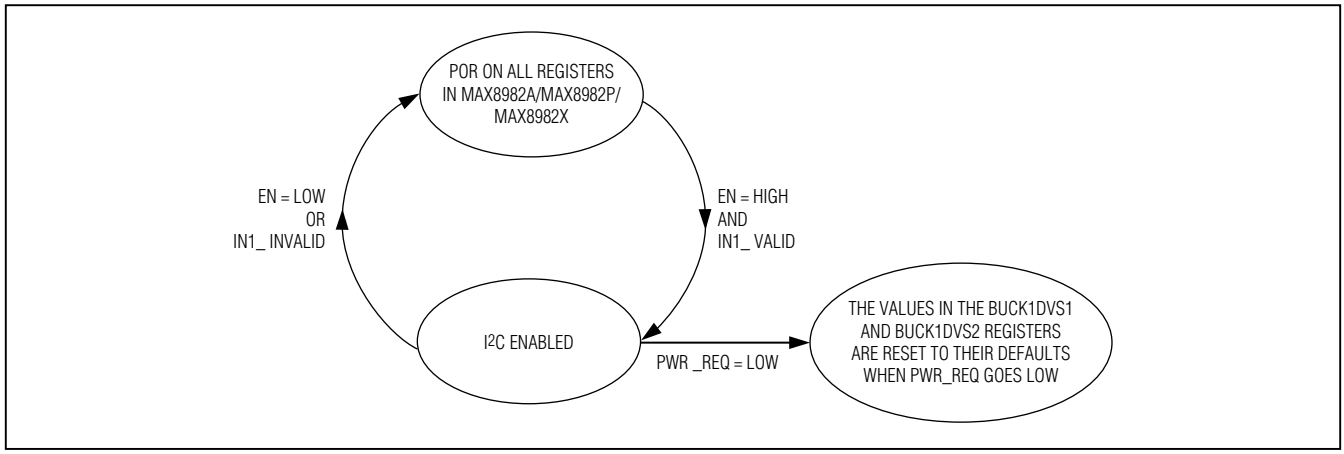


Figure 9. POR State Diagram

Current Regulators (DR1, DR2, DR3)

The ICs have three current regulators that can handle up to 24mA. The sink current for each current regulator is set from 3mA to 24mA in 3mA increments through I²C. The default set current is 24mA on each channel.

If a current other than the programmable options is required, a series resistor can be added to set a current from 0mA to 24mA (Figure 10). The resistor forces the current regulator to operate in dropout. Set the resistor value to ($V_{IN1\_}$ - V_F)/I_{LED}, where V_F is the forward voltage of the LED at the desired current and I_{LED} is the desired LED current. I_{LED} must be less than the programmed current (24mA default).

Each current regulator has an embedded flash timer. The flash time is programmable through the I²C interface. This feature allows the system designer to generate a desired pattern on LED.

Embedded Flash Timer

The flash generator is clocked by the internal 32kHz oscillator. It consists of a counter that wraps at a programmable value to provide a configurable sequence period (t_P). Up to four on-pulses can be programmed in this sequence and the start time for each pulse is programmed individually (t_1–t_4). The programmable LED on-time (t_{ON}) for each pulse is the same for each pulse. The flash timing is shown in Figure 11. The dimming current can be changed at any time.

$\overline{IRQ}$ Description

The ICs use the $\overline{IRQ}$ to indicate to the baseband processor that their status has changed. The $\overline{IRQ}$ signal is asserted (pulls low) whenever an interrupt is triggered. The baseband controller shall read the interrupt register to find sources of interrupt. $\overline{IRQ}$ is cleared (high) as soon as the read sequence of the last IRQ register that contains an active interrupt starts. If an interrupt is captured during the read sequence, $\overline{IRQ}$ becomes active (low) after minimum 24 cycles of the I²C clock. An interrupt can be masked to prevent $\overline{IRQ}$ from being asserted for the masked event. A mask bit in the IRQM register implements masking.

For UVLO interrupt bit, the bit status is only maintained as long as V_{BUS} is higher than 2.0V in any conditions.

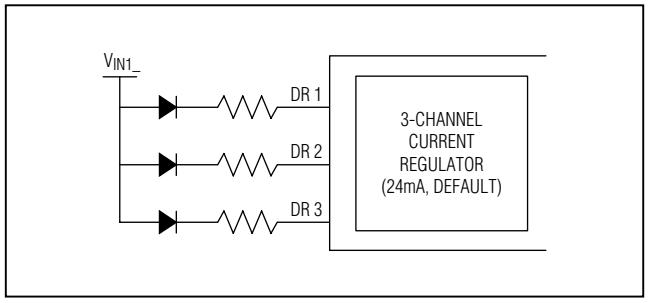


Figure 10. Adding Series Resistors to Adjust LED Current

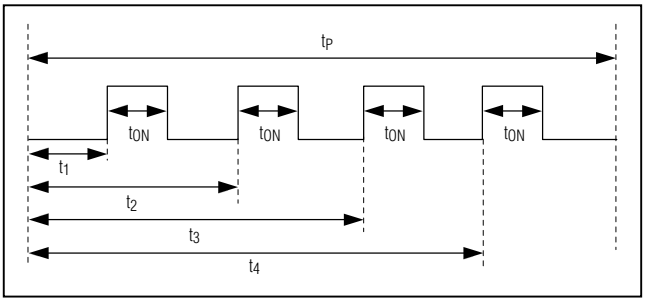


Figure 11. Flash Timing Diagram

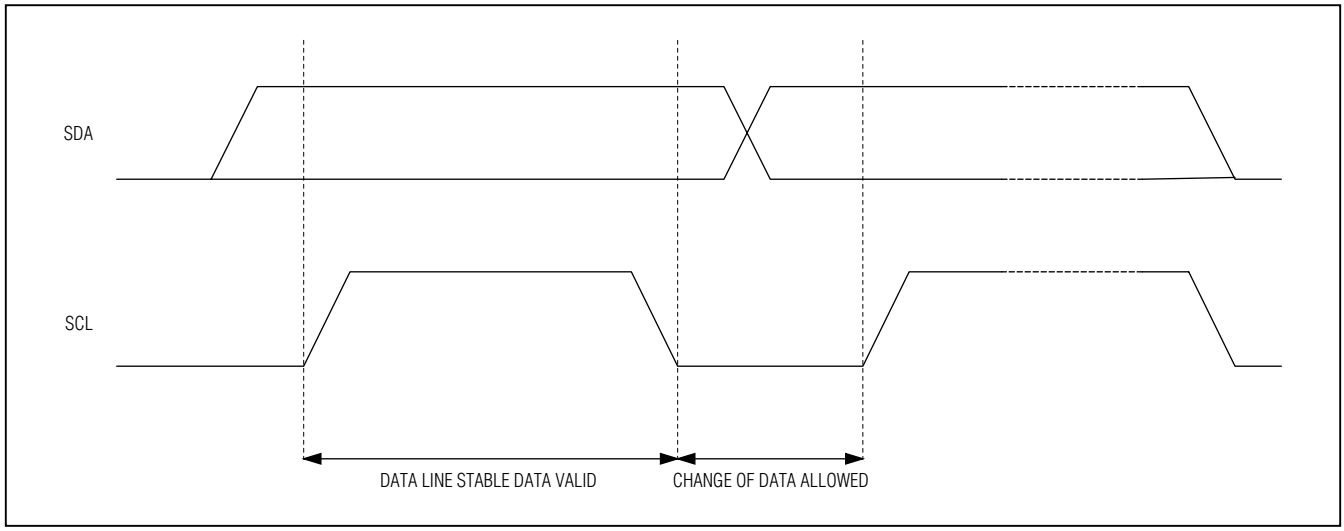


Figure 12. I²C Bit Transfer

$\overline{\text{RESET}}$ SIGNAL to B/B Chipset

The ICs include one dedicated reset output called $\overline{\text{RESET}}$. This is the reset signal for the core and RTB (real-time block) in baseband. $\overline{\text{RESET}}$ goes high after the ICs' power-up sequence is complete. $\overline{\text{RESET}}$ is pulled low when the ICs are shut down (due to input supply out of range or EN goes low).

I²C Serial Interface

An I²C-compatible, 2-wire serial interface is used for regulator on/off control, setting output voltages, LED control, and other functions. See Table 5 for the complete register map.

The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock line (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of the SCL clock pulse (Figure 12). Changes in SDA while SCL is high are control signals (START and STOP conditions).

START and STOP Conditions

Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each packet is 9 bits long; 8 bits of data followed by the acknowledge bit. The ICs support data transfer rates with a SCL frequency up to 400kHz.

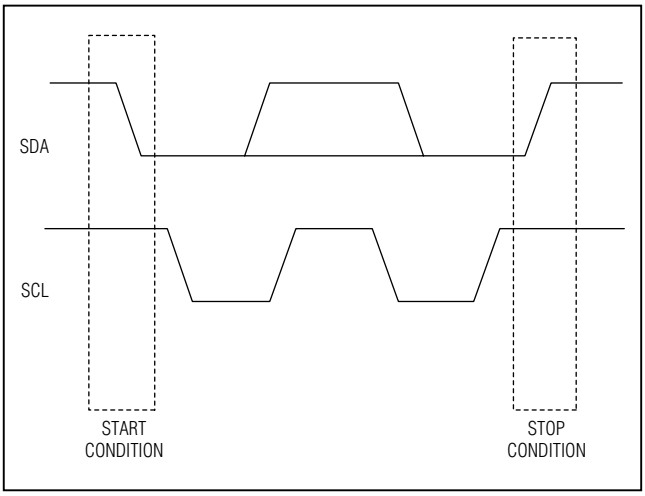


Figure 13. START and STOP Conditions

Both SDA and SCL remain high when the bus is not busy. The master device initiates communication by issuing a START condition. A START condition is a high-to-low transition of SDA, while SCL is high. A STOP condition is a low-to-high transition of the data line while SCL is high (Figure 13).

A START condition from the master signals the beginning of a transmission to the ICs. The master terminates transmission by issuing a not acknowledge followed by a STOP condition. See the *Acknowledge* section for more information. The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue

REPEATED START (Sr) commands instead of a STOP command to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the ICs internally disconnect SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

System Configuration

A device on the I²C bus that generates a message is called a transmitter, and a device that receives the message is a receiver. The device that controls the message is the master, and the devices that are controlled by the master are called slaves (Figure 14).

The ICs are slave transmitter/receiver devices, and the B/B chipset is a master transmitter/receiver. The master initiates data transfer on the bus and generates SCL to permit data transfer.

Acknowledge

The number of data bytes between the START and STOP conditions for the transmitter and receiver are unlimited. Each 8-bit byte is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on SDA by the transmitter during which time the master generates an extra acknowledge-related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter. See Figure 15.

The device that acknowledges must pull down the DATA line during the acknowledge clock pulse, so that the DATA line is stable low during the high period of the acknowledge clock pulse (setup and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a STOP condition.

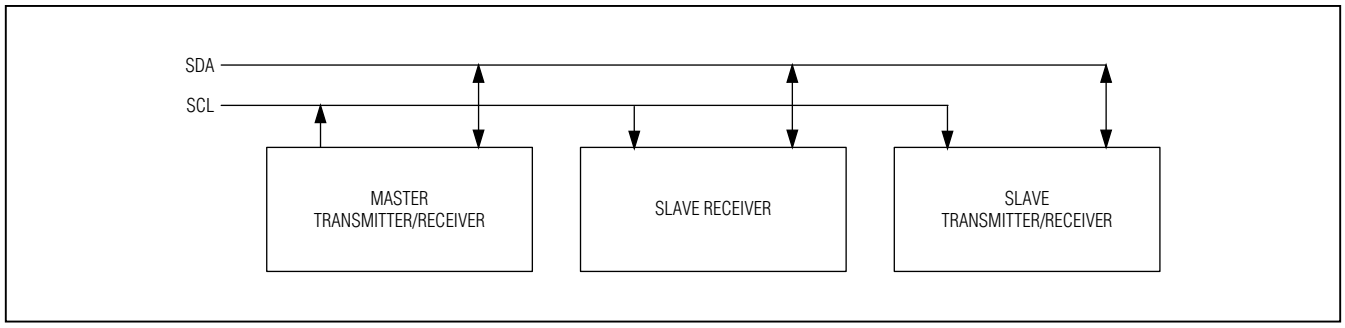


Figure 14. Master/Slave Configuration

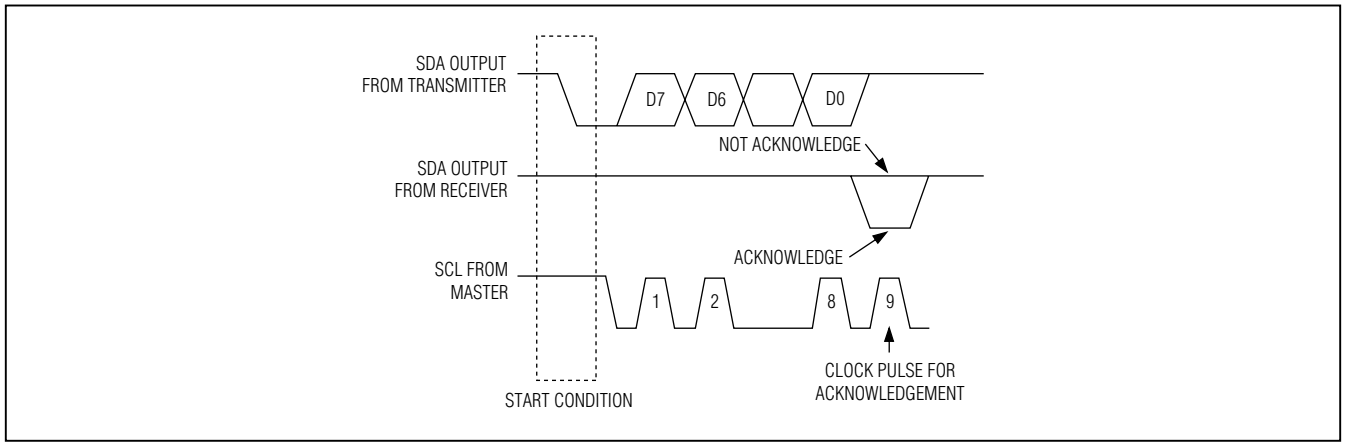


Figure 15. I²C Acknowledge

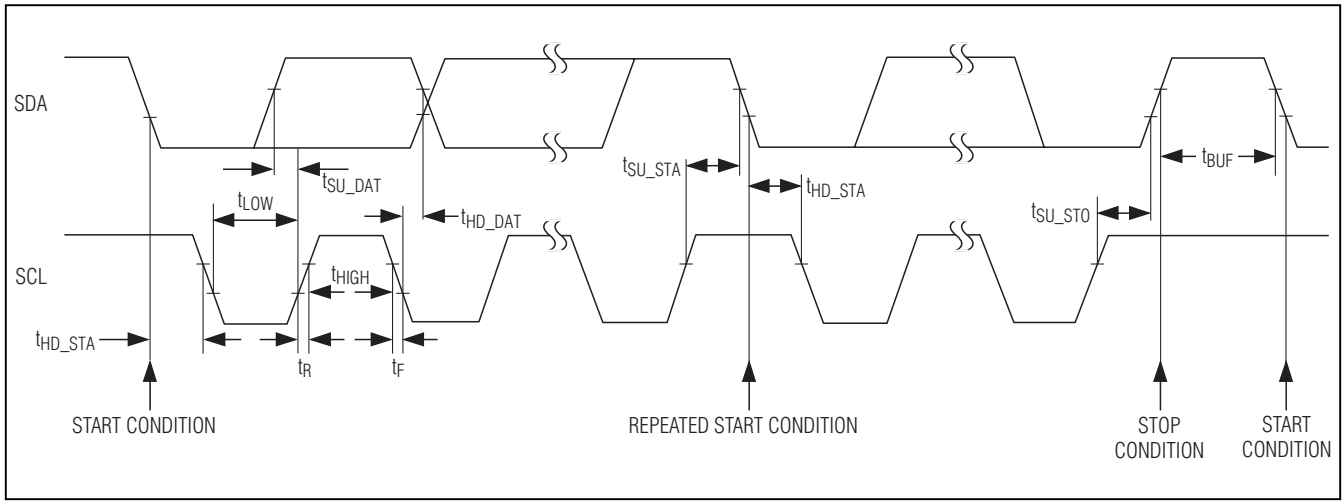


Figure 16. I²C Timing Diagram

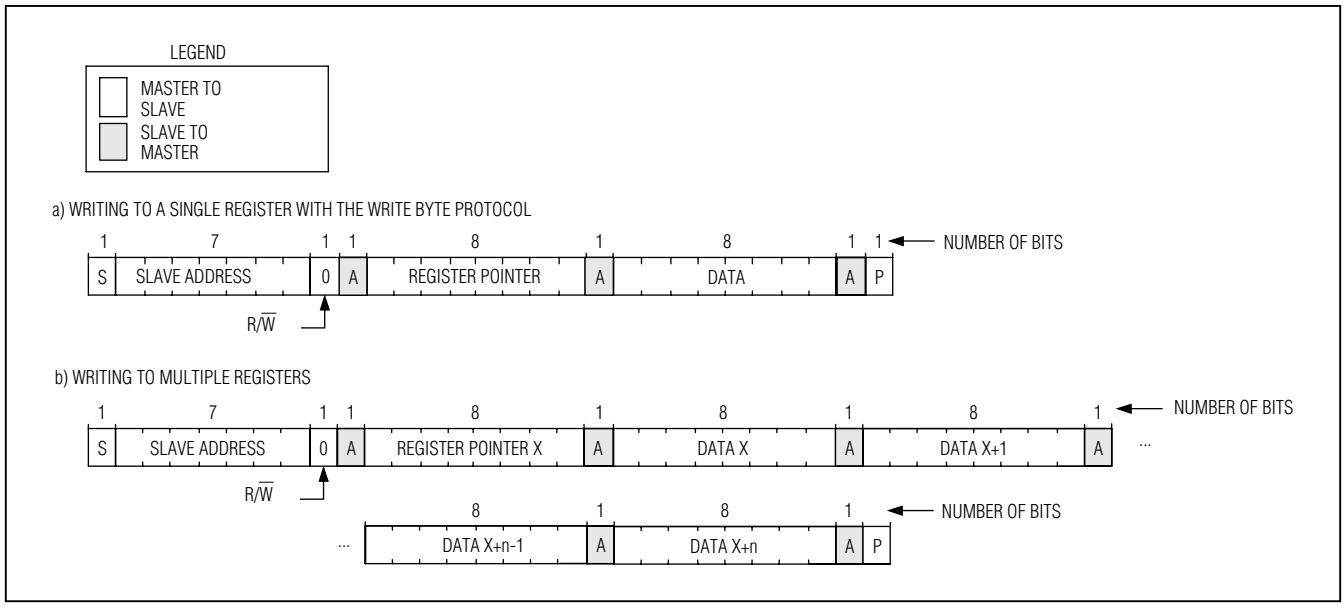


Figure 17. Writing to the ICs

Slave Address

The ICs act as a slave transmitter/receiver. The slave address of the ICs is:

10000010 (0x82) for write operations

10000011 (0x83) for read operations

The least significant bit is the read/write indicator.

1	0	0	0	0	0	1	R/$\overline{W}$

Write Operations

Use the following procedure to write to a sequential block of registers (Figure 17):

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit (0x82).
3) The addressed slave asserts an acknowledge by pulling SDA low.

4) The master sends the 8-bit register pointer of the first register to write.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte.
8) The slave updates with the new data.
9) Steps 6 to 8 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
10) The master sends a STOP condition.

Read Operations

Use the following method to read a sequential block of registers (Figure 18):

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit (0x83).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer of the first register in the block.
5) The slave acknowledges the register pointer.
6) The master sends a repeated START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave asserts an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master asserts an acknowledge by pulling SDA low when there is more data to read, or a not acknowledge by keeping SDA high when all data has been read.
11) Steps 9 and 10 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
12) The master sends a STOP condition.

The register pointer can be omitted from the above procedure when starting from register 0x00.

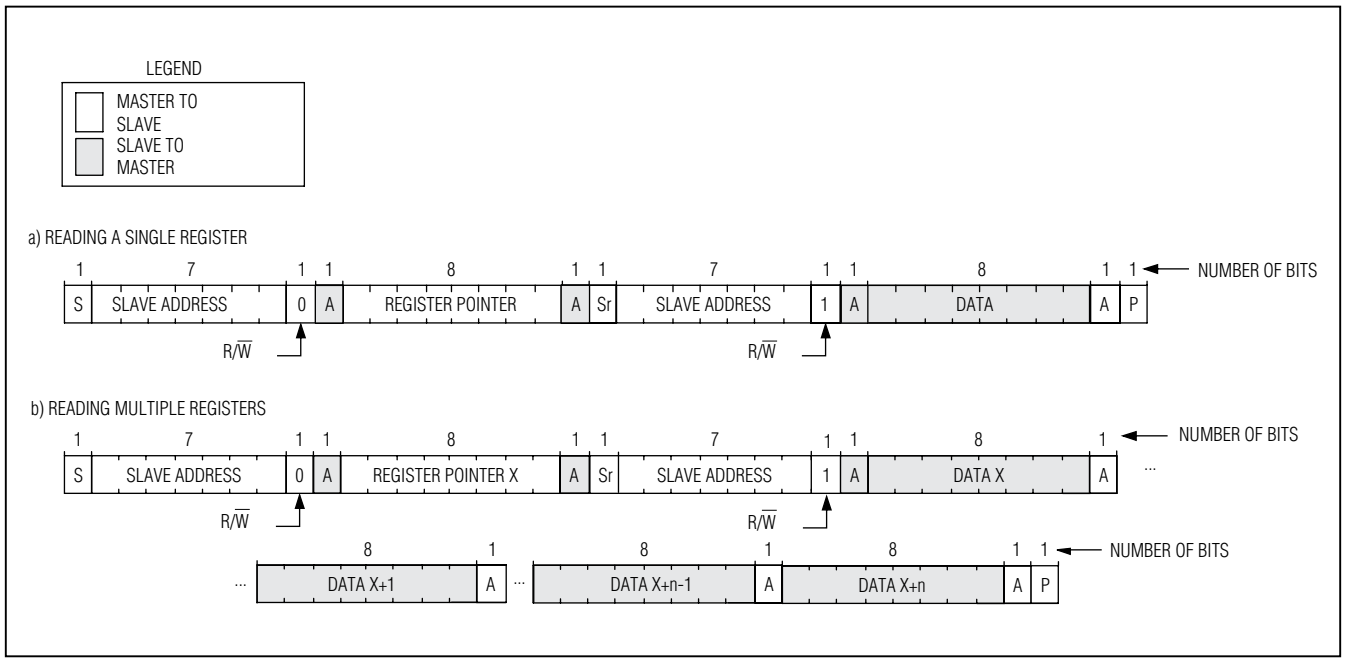


Figure 18. Reading from the ICs

Table 5. Register Map

ADDRESS (HEX)	POR (HEX)	R/W	NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
02	—	R	CHIPID	Reserved	Reserved	PASS[1:0]		Reserved	Reserved	Reserved	VOPTION
03	00	R/W	IRQM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UVLOFM	HIGHTMPM
13	00	R/W	IRQ	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UVLOF	HIGHTMP
14	N/A	R	STATUS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UVLOF	HIGHTMP
18	00	R/W	LED1FT1	Reserved	Reserved	Reserved	FLASHEN	LD1TON[3:0]			
19	00	R/W	LED1FT2	Reserved	LD1T1[6:0]						
1A	00	R/W	LED1FT3	Reserved	LD1T2[6:0]						
1B	00	R/W	LED1FT4	Reserved	LD1T3[6:0]						
1C	00	R/W	LED1FT5	Reserved	LD1T4[6:0]						
1D	00	R/W	LED1FT6	Reserved	LD1TP[6:0]						
20	00	R/W	LED2FT1	Reserved	Reserved	Reserved	FLASHEN	LD2TON[3:0]			
21	00	R/W	LED2FT2	Reserved	LD2T1[6:0]						
22	00	R/W	LED2FT3	Reserved	LD2T2[6:0]						
23	00	R/W	LED2FT4	Reserved	LD2T3[6:0]						
24	00	R/W	LED2FT5	Reserved	LD2T4[6:0]						
25	00	R/W	LED2FT6	Reserved	LD2TP[6:0]						
28	00	R/W	LED3FT1	Reserved	Reserved	Reserved	FLASHEN	LD3TON[3:0]			
29	00	R/W	LED3FT2	Reserved	LD3T1[6:0]						
2A	00	R/W	LED3FT3	Reserved	LD4T2[6:0]						
2B	00	R/W	LED3FT4	Reserved	LD4T3[6:0]						
2C	00	R/W	LED3FT5	Reserved	LD4T4[6:0]						
2D	00	R/W	LED3FT6	Reserved	LD4TP[6:0]						
3D	47	R/W	BUCK1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BUCK1[1:0]	
3F	0C	R/W	BUCK1DVS1	Reserved	Reserved	Reserved	SD1[4:0]				
40	0C	R/W	BUCK1DVS2	Reserved	Reserved	Reserved	SD1[4:0]				
45	45	R/W	BUCK2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BUCK2[1:0]	
4C	03	R/W	LDO1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO1[1:0]	
4D	04	R/W	LDO1V	Reserved	Reserved	Reserved	L1[4:0]				
4E	03	R/W	LDO2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO2[1:0]	
4F	04	R/W	LDO2V	Reserved	Reserved	Reserved	L2[4:0]				
50	01	R/W	LDO3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO3[1:0]	
51	07	R/W	LDO3V	Reserved	Reserved	Reserved	L3[4:0]				
52	03	R/W	LDO4	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO4[1:0]	
53	00	R/W	LDO4V	Reserved	Reserved	Reserved	L4[4:0]				
54	00	R/W	LDO5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO5[1:0]	
55	07	R/W	LDO5V	Reserved	Reserved	Reserved	L5[4:0]				
56	01	R/W	LDO6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO6[1:0]	
57	07	R/W	LDO6V	Reserved	Reserved	Reserved	L6[4:0]				
58	00	R/W	VSIM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO7[1:0]	
59	0B	R/W	VSIMV	Reserved	Reserved	Reserved	L7[4:0]				

Table 5. Register Map (continued)

ADDRESS (HEX)	POR (HEX)	R/W	NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
5A	01	R/W	LDO8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO8[1:0]	
5B	06	R/W	LDO8V	Reserved	Reserved	Reserved	L8[4:0]				
5C	01	R/W	LDO9	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO9[1:0]	
5D	00	R/W	LDO9V	Reserved	Reserved	Reserved	L9[4:0]				
6B	00	R/W	LED_EN	Reserved	Reserved	Reserved	Reserved	Reserved	LED3EN	LED2EN	LED1EN
70	03	R/W	ON/OFF	Reserved	Reserved	Reserved	BUCK4[1:0]		BUCK3[1:0]		32KCLK
72	06	R/W	BUCK3	Reserved	Reserved	Reserved	Reserved	SD3[3:0]			
73	08	R/W	BUCK4	Reserved	Reserved	Reserved	Reserved	SD4[3:0]			
75	3F	R/W	CURRENTREG1	Reserved	Reserved	DR1[2:0]			DR2[2:0]		
76	07	R/W	CURRENTREG2	Reserved	Reserved	Reserved	Reserved	Reserved	DR3[2:0]		
77	02	R/W	RAMP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RASD1[1:0]	
78	04	R/W	BUCK1-4ADIS	Reserved	Reserved	Reserved	Reserved	SD1ADIS	SD2ADIS	SD3ADIS	SD4ADIS
79	00	R/W	LDO1-8ADIS	LDO1ADIS	LDO2ADIS	LDO3ADIS	LDO4ADIS	LDO5ADIS	LDO6ADIS	LDO7ADIS	LDO8ADIS
7A	00	R/W	LDO9ADIS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO9ADIS

Table 6. CHIPID Register

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
02	—	R	Reserved	Reserved	PASS[1:0]		Reserved	Reserved	Reserved	VOPTION

NAME	POR	DESCRIPTION
VOPTION	—	0: 5V input option (MAX8982A) 1: 3.3V input option (MAX8982X/MAX8982P)
PASS[1:0]	—	Chip revision version

Table 7. IRQM Register (Interrupt Mask)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
03	00	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UVLOFM	HIGH TMPM

NAME	POR	DESCRIPTION
HIGH TMPM	0	**0: Interrupt enabled.** 1: Mask HIGHTMP interrupt.
UVLOFM	0	**0: Interrupt enabled.** 1: Mask UVLOF interrupt.

Note: *The IRQM register is effective only as long as IN1A and IN1B are higher than the falling UVLO threshold. If the IN1A and IN1B are below the falling UVLO threshold, this IRQM register resets to the POR value.*

Table 8. IRQ Register

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
13	00	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UVLOF	HIGH TMP

NAME	POR	DESCRIPTION
HIGH TMP	0	**0: No high temperature event detected.** 1: Temperature sensor detects +125°C.
UVLOF	0	**0: No UVLO event detected.** 1: UVLO falling is detected.

Note: *The IRQ register is effective only as long as IN1A and IN1B are higher than 2.0V. If the IN1A and IN1B are below 2.0V, these registers reset to the POR value.*

Table 9. STATUS Register

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
14	N/A	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UVLOF	HIGH TMP

NAME	POR	DESCRIPTION
HIGHTMP	—	0: T_J < +125°C 1: T_J > +125°C
UVLOF	—	0: Falling UVLO threshold is not detected. 1: Falling UVLO threshold is detected.

Table 10. LED1FT1 Register (LED1 (DR1) Flash Timer On/Off and TON Adjust)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
18	00	R/W	Reserved	Reserved	Reserved	FLASHEN	LD1TON[3:0]			

NAME	POR	DESCRIPTION
FLASHEN	0	1: Flasher is enabled. **0: Flasher is disabled.**

LD1TON[3:0]	0000	BIT 3	BIT 2	BIT 1	BIT 0	t_{ON} (ms)
		0	0	0	0	25
		0	0	0	1	50
		. .	. .	. .	. .	. .
		1	1	1	1	400
		From 25ms to 400ms in 25ms increments.				

Table 11. LED1FT2 Register (LED1 (DR1) Flash Timer t_1 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
19	00	R/W	Reserved	LD1T1[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD1T1[0:6]	0000000		**BIT**							**t_1 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 12. LED1FT3 Register (LED1 (DR1) Flash Timer t_2 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1A	00	R/W	Reserved	LD1T2[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD1T2[0:6]	0000000		**BIT**							**t_2 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	0	25
			0	0	0	0	0	1	0	50
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 13. LED1FT4 Register (LED1 (DR1) Flash Timer t_3 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1B	00	R/W	Reserved	LD1T3[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD1T3[6:0]	0000000		**BIT**							**t_3 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 14. LED1FT5 Register (LED1 (DR1) Flash Timer t_4 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1C	00	R/W	Reserved	LD1T4[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD1T4[6:0]	0000000		**BIT**							**t_4 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 15. LED1FT6 Register (LED1 (DR1) Flash Timer t_P Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1D	00	R/W	Reserved	LD1TP[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD1TP[6:0]	0000000		**BIT**							**t_P TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			0	0	0	0	0	1	1	75
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 16. LED2FT1 Register (LED2 (DR2) Flash Timer On/Off and t_{ON} Adjust)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
20	00	R/W	Reserved	Reserved	Reserved	Flash EN	LD2TON[3:0]			
NAME	**POR**		**DESCRIPTION**							
LD2TON[3:0]	0000		1: Flasher is enabled. **0: Flasher is disabled.**							
			BIT				**t_{ON} TIME (ms)**			
			3	2	1	0				
			0	0	0	0	25			
			0	0	0	1	50			
			. .	. .	. .	. .	. .			
			1	1	1	1	400			
			From 25ms to 400ms in 25ms increments.							

Table 17. LED2FT2 Register (LED2 (DR2) Flash Timer t_1 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
21	00	R/W	Reserved	LD2T1[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD2T1[6:0]	0000000		**BIT**							**t_1 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 18. LED2FT3 Register (LED2 (DR2) Flash Timer t_2 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
22	00	R/W	Reserved	LD2T2[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD2T2[6:0]	0000000		**BIT**							**t_2 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 19. LED2FT4 Register (LED2 (DR2) Flash Timer t_3 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
23	00	R/W	Reserved	LD2T3[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD2T3[6:0]	0000000		**BIT**							**t_3 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 20. LED2FT5 Register (LED2 (DR2) Flash Timer t_4 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
24	00	R/W	Reserved	LD2T4[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD2T4[6:0]	0000000		**BIT**							**t_4 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 21. LED2FT6 Register (LED2 (DR2) Flash Timer t_P Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
25	00	R/W	Reserved	LD2TP[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD2TP[6:0]	0000000		**BIT**							**t_P TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 22. LED3FT1 Register (LED3 (DR3) Flash Timer On/Off and t_{ON} Adjust)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
28	00	R/W	Reserved	Reserved	Reserved	FLASHEN	LD3TON[3:0]			
NAME	**POR**		**DESCRIPTION**							
FLASHEN	0		1: Flasher is enabled. **0: Flasher is disabled.**							
LD3TON[3:0]	0000		**BIT**				**t_{ON} TIME (ms)**			
			3	2	1	0				
			0	0	0	0	25			
			0	0	0	1	50			
			. .	. .	. .	. .	. .			
			1	1	1	1	400			
			From 25ms to 400ms in 25ms increments.							

Table 23. LED3FT2 Register (LED3 (DR3) Flash Timer t_1 Setting

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
29	00	R/W	Reserved	LD3T1[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD3T1[6:0]	0000000		**BIT**							**t_1 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 24. LED3FT3 Register (LED3 (DR3) Flash Timer t_2 Setting)

ADRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
2A	00	R/W	Reserved	LD3T2[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD3T2[6:0]	0000000		**BIT**							**t_2 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 25. LED3FT4 Register (LED3 (DR3) Flash Timer t_3 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
2B	00	R/W	Reserved	LD3T3[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD3T3[6:0]	0000000		**BIT**							**t_3 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 26. LED3FT5 Register (LED3 (DR3) Flash Timer t_4 Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
2C	00	R/W	Reserved	LD3T4[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD3T4[6:0]	0000000		**BIT**							**t_4 TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 27. LED3FT6 Register (LED3 (DR3) Flash Timer t_P Setting)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
2D	00	R/W	Reserved	LD3TP[6:0]						
NAME	**POR**		**DESCRIPTION**							
LD3TP[6:0]	0000000		**BIT**							**t_P TIME (ms)**
			6	5	4	3	2	1	0	
			0	0	0	0	0	0	0	0
			0	0	0	0	0	0	1	25
			0	0	0	0	0	1	0	50
			0	0	0	0	0	1	1	75
			. .	. .	. .	. .	. .	. .	. .	. .
			1	1	1	1	1	1	1	3175
			From 0ms to 3175ms in 25ms increments.							

Table 28. BUCK1 Register (On/Off Control for BUCK1)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3D	47	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BUCK1[1:0]	
BITS 7:2			**Reserved, write 010001 to these bits.**							
BIT 1	**BIT 0**		**DESCRIPTION**							
0	0		BUCK1 off (in I^2C on mode).							
0	1		BUCK1 on (in I^2C on mode).							
1	0		BUCK1 on (in PWR_REQ on mode) (Group D).							
1	**1**		**BUCK1 on (in PWR_REQ on mode) (Group D).**							

Table 29. BUCK1DVS1 Register (Output Voltage Setting for BUCK1 (DVS1 = Low))

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3F	0C	R/W	Reserved	Reserved	Reserved	SD1[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							
DESCRIPTION										
BIT 4	**BIT 3**		**BIT 2**		**BIT 1**		**BIT 0**		**V_{PROG} (V)**	
0	0		0		0		0		0.600	
0	0		0		0		1		0.625	
0	0		0		1		0		0.650	
0	0		0		1		1		0.675	
0	0		1		0		0		0.700	
0	0		1		0		1		0.725	
0	0		1		1		0		0.750	
0	0		1		1		1		0.775	
0	1		0		0		0		0.800	
0	1		0		0		1		0.825	
0	1		0		1		0		0.850	
0	1		0		1		1		0.875	
0	**1**		**1**		**0**		**0**		**0.900**	
0	1		1		0		1		0.925	
0	1		1		1		0		0.950	
0	1		1		1		1		0.975	
1	0		0		0		0		1.000	
1	0		0		0		1		1.025	
1	0		0		1		0		1.050	
1	0		0		1		1		1.075	
1	0		1		0		0		1.100	
1	0		1		0		1		1.125	
1	0		1		1		0		1.150	
1	0		1		1		1		1.175	
1	1		X		X		X		1.200	

X = Don't care.

Table 30. BUCK1DVS2 Register (Output Voltage Setting for BUCK1 (DVS1 = High))

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
40	0C	R/W	Reserved	Reserved	Reserved	SD1[4:0]				
BITS 7:5		**Reserved, write 000 to these bits.**								
DESCRIPTION										
BIT 4	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**					
0	0	0	0	0	0.600					
0	0	0	0	1	0.625					
0	0	0	1	0	0.650					
0	0	0	1	1	0.675					
0	0	1	0	0	0.700					
0	0	1	0	1	0.725					
0	0	1	1	0	0.750					
0	0	1	1	1	0.775					
0	1	0	0	0	0.800					
0	1	0	0	1	0.825					
0	1	0	1	0	0.850					
0	1	0	1	1	0.875					
0	**1**	**1**	**0**	**0**	**0.900**					
0	1	1	0	1	0.925					
0	1	1	1	0	0.950					
0	1	1	1	1	0.975					
1	0	0	0	0	1.000					
1	0	0	0	1	1.025					
1	0	0	1	0	1.050					
1	0	0	1	1	1.075					
1	0	1	0	0	1.100					
1	0	1	0	1	1.125					
1	0	1	1	0	1.150					
1	0	1	1	1	1.175					
1	1	X	X	X	1.200					

X = Don't care.

Table 31. BUCK2 Register (On/Off Control for BUCK2)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
45	45	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BUCK2[1:0]	
BITS 7:2			**Reserved, write 010001 to these bits.**							
BIT 1	**BIT 0**		**DESCRIPTION**							
0	0		BUCK2 off (in I²C on mode).							
0	**1**		**BUCK2 on (in I²C on mode).**							
1	0		BUCK2 on (in PWR_REQ on mode) (Group A).							
1	1		BUCK2 on (in PWR_REQ on mode) (Group A).							

Table 32. LDO1 Register (On/Off Control for LDO1)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4C	03	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO1[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							
BIT 1	**BIT 0**		**DESCRIPTION**							
0	0		LDO1 off (in I²C on mode).							
0	1		LDO1 on (in I²C on mode).							
1	0		LDO1 on (in PWR_REQ on mode) (Group B).							
1	**1**		**LDO1 on (in PWR_REQ on mode) (Group B).**							

Table 33. LDO1V Register (Output Voltage Setting for OUT1)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4D	04	R/W	Reserved	Reserved	Reserved	L1[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							
DESCRIPTION										
BIT 4	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**					
0	0	0	0	0	2.65					
0	0	0	0	1	2.65					
0	0	0	1	0	2.65					
0	0	0	1	1	2.65					
0	**0**	**1**	**0**	**0**	**2.70**					
0	0	1	0	1	2.70					
0	0	1	1	0	2.75					
0	0	1	1	1	2.80					
0	1	0	0	0	2.85					
0	1	0	0	1	2.90					
0	1	0	1	0	2.95					
0	1	0	1	1	3.00					
0	1	1	X	X	3.00					
1	X	X	X	X	3.00					

X = Don't care.

Table 34. LDO2 Register (ON/OFF Control for LDO2)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4E	03	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO2[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							
BIT 1	**BIT 0**		**DESCRIPTION**							
0	0		LDO2 off (in I²C on mode).							
0	1		LDO2 on (in I²C on mode).							
1	0		LDO2 on (in PWR_REQ on mode) (Group A).							
1	**1**		**LDO2 on (in PWR_REQ on mode) (Group A).**							

Table 35. LDO2V Register (Output Voltage Setting for OUT2)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
4F	04	R/W	Reserved	Reserved	Reserved	L2[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							
DESCRIPTION										
BIT 4	**BIT 3**		**BIT 2**		**BIT 1**		**BIT 0**		**V_{PROG} (V)**	
0	0		0		0		0		1.50	
0	0		0		0		1		1.50	
0	0		0		1		0		1.50	
0	0		0		1		1		1.50	
0	**0**		**1**		**0**		**0**		**1.80**	
0	0		1		0		1		2.70	
0	0		1		1		0		2.70	
0	0		1		1		1		2.70	
0	1		0		0		0		2.70	
0	1		0		0		1		2.70	
0	1		0		1		0		2.70	
0	1		0		1		1		1.70	
0	1		1		X		X		1.70	
1	X		X		X		X		1.70	

X = Don't care.

Table 36. LDO3 Register (On/Off Control for LDO3)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
50	01	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO3[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							
BIT 1	**BIT 0**		**DESCRIPTION**							
0	0		LDO3 off (in I²C on mode).							
0	**1**		**LDO3 on (in I²C on mode).**							
1	0		LDO3 on (in PWR_REQ on mode) (Group B).							
1	1		LDO3 on (in PWR_REQ on mode) (Group B).							

Table 37. LDO3V Register (Output Voltage Setting for OUT3)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
51	07	R/W	Reserved	Reserved	Reserved	L3[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							

DESCRIPTION					
BIT 4	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**
0	0	0	0	0	2.65
0	0	0	0	1	2.65
0	0	0	1	0	2.65
0	0	0	1	1	2.65
0	0	1	0	0	2.70
0	0	1	0	1	2.70
0	0	1	1	0	2.75
0	**0**	**1**	**1**	**1**	**2.80**
0	1	0	0	0	2.85
0	1	0	0	1	2.90
0	1	0	1	0	2.95
0	1	0	1	1	3.00
0	1	1	X	X	3.00
1	X	X	X	X	3.00

X = Don't care.

Table 38. LDO4 Register (On/Off Control for LDO4)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
52	03	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO4[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							

BIT 1	BIT 0	DESCRIPTION
0	0	LDO4 off (in I^2C on mode).
0	1	LDO4 on (in I^2C on mode).
1	0	LDO4 on (in PWR_REQ on mode) (Group D).
1	**1**	**LDO4 on (in PWR_REQ on mode) (Group D).**

Table 39. LDO4V Register (Output Voltage Setting for OUT4)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
53	00	R/W	Reserved	Reserved	Reserved	L4[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							

DESCRIPTION					
BIT 4	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**
0	**0**	**0**	**0**	**0**	**0.90**
0	0	0	0	1	1.00
0	0	0	1	0	1.20
0	0	0	1	1	1.10
X	X	1	X	X	0.80
X	1	X	X	X	0.80
1	X	X	X	X	0.80

X = Don't care.

Table 40. LDO5 Register (On/Off Control for LDO5)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
54	00	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO5[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							

BIT 1	BIT 0	DESCRIPTION
0	**0**	**LDO5 off (in I^2C on mode).**
0	1	LDO5 on (in I^2C on mode).
1	0	LDO5 on (in PWR_REQ on mode) (Group C).
1	1	LDO5 on (in PWR_REQ on mode) (Group C).

Table 41. LDO5V Register (Output Voltage Setting for OUT5)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
55	07	R/W	Reserved	Reserved	Reserved	L5[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							

DESCRIPTION					
BIT 4	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**
0	0	0	0	0	3.20
0	0	0	0	1	3.20
0	0	0	1	0	3.20
0	0	0	1	1	3.20
0	0	1	0	0	3.20
0	0	1	0	1	2.80
0	0	1	1	0	2.80
0	**0**	**1**	**1**	**1**	**3.00**
0	1	0	0	0	3.00
0	1	0	0	1	2.90
0	1	0	1	0	2.90
0	1	0	1	1	3.00
0	1	1	X	X	3.00
1	X	X	X	X	3.00

X = Don't care.

Table 42. LDO6 Register (On/Off Control for LDO6)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
56	01	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO6[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							

BIT 1	**BIT 0**	**DESCRIPTION**
0	0	LDO6 on (in PWR_REQ on mode) (Group C).
0	**1**	**LDO6 on (in PWR_REQ on mode) (Group C).**
1	0	LDO6 off (in I^2C off mode).
1	1	LDO6 on (in I^2C on mode).

Note: *The enable mapping for LDO6 is different from all other LDOs.*

Table 43. LDO6V Register (Output Voltage Setting for OUT6)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
57	07	R/W	Reserved	Reserved	Reserved	L6[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							

DESCRIPTION					
BIT 4	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**
0	0	0	0	0	2.65
0	0	0	0	1	2.65
0	0	0	1	0	2.65
0	0	0	1	1	2.65
0	0	1	0	0	2.65
0	0	1	0	1	2.70
0	0	1	1	0	2.70
0	**0**	**1**	**1**	**1**	**2.70**
0	1	0	0	0	2.75
0	1	0	0	1	2.80
0	1	0	1	0	2.85
0	1	0	1	1	2.90
0	1	1	0	0	2.95
0	1	1	0	1	3.00
0	1	1	1	X	3.00
1	X	X	X	X	3.00

X = Don't care.

Table 44. VSIM Register (On/Off Control for VSIM (LDO7))

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
58	00	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO7[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							

BIT 1	BIT 0	DESCRIPTION
0	**0**	**LDO7 off (in I^2C off mode).**
0	1	LDO7 on (in I^2C on mode).
1	0	LDO7 on (in PWR_REQ on mode) (Group C).
1	1	LDO7 on (in PWR_REQ on mode) (Group C).

Table 45. VSIMV Register (Output Voltage Setting for VSIM)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
59	0B	R/W	Reserved	Reserved	Reserved	L7[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							

DESCRIPTION					
BIT 4	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**
0	0	0	0	0	1.80
0	0	0	0	1	1.80
0	0	0	1	0	1.80
0	0	0	1	1	1.80
0	0	1	0	0	1.80
0	0	1	0	1	1.80
0	0	1	1	0	1.80
0	0	1	1	1	1.80
0	1	0	0	0	1.80
0	1	0	0	1	1.80
0	1	0	1	0	1.80
0	**1**	**0**	**1**	**1**	**3.00**
0	1	1	X	X	3.00
1	X	X	X	X	3.00

X = Don't care.

Table 46. LDO8 Register (On/Off Control for LDO8)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5A	01	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO8[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							

BIT 1	BIT 0	DESCRIPTION
0	0	LDO8 off (in I²C off mode).
0	**1**	**LDO8 on (in I²C on mode).**
1	0	LDO8 on (in PWR_REQ on mode) (Group C).
1	1	LDO8 on (in PWR_REQ on mode) (Group C).

Note: *This register is not used by the MAX8982X.*

Table 47. LDO8V Register (Output Voltage Setting for OUT8)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5B	06	R/W	Reserved	Reserved	Reserved	L8[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							

DESCRIPTION					
BIT 4	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**
0	0	0	0	0	3.00
0	0	0	0	1	3.00
0	0	0	1	0	3.00
0	0	0	1	1	3.00
0	0	1	0	0	3.00
0	0	1	0	1	3.00
0	**0**	**1**	**1**	**0**	**3.00**
0	0	1	1	1	3.10
0	1	0	0	0	3.20
0	1	0	0	1	3.20
0	1	0	1	0	3.20
0	1	0	1	1	3.20
0	1	1	0	0	3.20
0	1	1	0	1	3.20
0	1	1	1	0	3.20
0	1	1	1	1	3.20
1	0	0	0	0	3.20
1	0	0	0	1	3.20
1	0	0	1	X	3.30
1	0	1	X	X	3.30
1	1	X	X	X	3.30

Note: *This register is not used by the MAX8982X.*
X = Don't care.

Table 48. LDO9 Register (On/Off Control for LDO9)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5C	01	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO9[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							

BIT 1	BIT 0	DESCRIPTION
0	0	LDO9 off (in I^2C off mode).
0	**1**	**LDO9 on (in I^2C on mode).**
1	0	LDO9 on (in PWR_REQ on mode) (Group D).
1	1	LDO9 on (in PWR_REQ on mode) (Group D).

Table 49. LDO9V Register (Output Voltage Setting for OUT9)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5D	00	R/W	Reserved	Reserved	Reserved	L9[4:0]				
BITS 7:5			**Reserved, write 000 to these bits.**							

DESCRIPTION					
BIT 4	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**
0	**0**	**0**	**0**	**0**	**0.90**
0	0	0	0	1	1.00
0	0	0	1	0	1.20
0	0	0	1	1	1.10
X	X	1	X	X	0.80
X	1	X	X	X	0.80
1	X	X	X	X	0.80

X = Don't care.

Table 50. LED_EN Register (On/Off Control for 3 Current Regulators)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
6B	00	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	LED3 EN	LED2 EN	LED1 EN

NAME	POR	DESCRIPTION
LED3EN	0	1: Turn on LED3. **0: Turn off LED3.**
LED2EN	0	1: Turn on LED2. **0: Turn off LED2.**
LED1EN	0	1: Turn on LED1. **0: Turn off LED1.**

Table 51. On/Off Register (On/Off Control for BUCK3, BUCK4, and the Internal 32kHz Clock)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
70	03	R/W	Reserved	Reserved	Reserved	BUCK4[1:0]		BUCK3[1:0]		32KCLK

BITS 7:5	Reserved, write 000 to these bits.
NAME	**DESCRIPTION**
BUCK4[1] **BUCK4[0]**	
0 **0**	**BUCK4 off (in I²C on mode).**
0 1	BUCK4 on (in I²C on mode).
1 0	BUCK4 on (in PWR_REQ on mode) (Group B).
1 1	BUCK4 on (in PWR_REQ on mode) (Group B).
BUCK3[1] **BUCK3[0]**	**DESCRIPTION**
0 0	BUCK3 OFF (in I²C on mode).
0 **1**	**BUCK3 ON (in I²C on mode).**
1 0	BUCK3 ON (in PWR_REQ on mode).
1 1	BUCK3 ON (in PWR_REQ on mode).
NAME **POR**	**DESCRIPTION**
32KCLK **1**	**1: Turn on 32kHz.** 0: Turn off 32kHz.

Note: *The BUCK3 and BUCK4 bits are not used by the MAX8982X.*

Table 52. BUCK3 Register (Output Voltage Setting for BUCK3)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
72	06	R/W	Reserved	Reserved	Reserved	Reserved	SD3[3:0]			

BITS 7:4	Reserved, write 0000 to these bits.

DESCRIPTION				
BIT 3	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**
0	0	0	0	2.90
0	0	0	1	2.95
0	0	1	0	3.00
0	0	1	1	3.05
0	1	0	0	3.10
0	1	0	1	3.15
0	**1**	**1**	**0**	**3.20**
0	1	1	1	3.25
1	0	0	0	3.30
1	0	0	1	3.35
1	0	1	0	3.40
1	0	1	1	3.45
1	1	0	0	3.50
1	1	0	1	3.55
1	1	1	0	3.60
1	1	1	1	3.65

Note: *This register is not used by the MAX8982X.*

Table 53. BUCK4 Register (Output Voltage Setting for BUCK4)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
73	08	R/W	Reserved	Reserved	Reserved	Reserved	SD4[3:0]			
BITS 7:4			**Reserved, write 0000 to these bits.**							

DESCRIPTION				
BIT 3	**BIT 2**	**BIT 1**	**BIT 0**	**V_{PROG} (V)**
0	0	0	0	3.00
0	0	0	1	3.05
0	0	1	0	3.10
0	0	1	1	3.15
0	1	0	0	3.20
0	1	0	1	3.25
0	1	1	0	3.30
0	1	1	1	3.35
1	**0**	**0**	**0**	**3.40**
1	0	0	1	3.45
1	0	1	0	3.50
1	0	1	1	3.55
1	1	0	0	3.60
1	1	0	1	3.65
1	1	1	0	3.70
1	1	1	1	3.75

Note: *This register is not used by the MAX8982X.*

Table 54. CURRENTREG1 Register (Current Setting for Current Regulators DR1 and DR2)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
75	3F	R/W	Reserved	Reserved	DR1[2:0]			DR2[2:0]		
BITS 7:6			**Reserved, write 00 to these bits.**							
DESCRIPTION										
DR1[2]			**DR1[1]**		**DR1[0]**			**$I_{DR1\ PROG}$ (mA)**		
0			0		0			3		
0			0		1			6		
0			1		0			9		
0			1		1			12		
1			0		0			15		
1			0		1			18		
1			1		0			21		
1			**1**		**1**			**24**		
DR2[2]			**DR2[1]**		**DR2[0]**			**$I_{DR2\ PROG}$ (mA)**		
0			0		0			3		
0			0		1			6		
0			1		0			9		
0			1		1			12		
1			0		0			15		
1			0		1			18		
1			1		0			21		
1			**1**		**1**			**24**		

Table 55. CURRENTREG2 Register (Current Setting for Current Regulator DR3)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
76	07	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	DR3[2:0]		
BITS 7:3			**Reserved, write 00000 to these bits.**							
DESCRIPTION										
DR3[2]			**DR3[1]**		**DR3[0]**			**$I_{DR3\ PROG}$ (mA)**		
0			0		0			3		
0			0		1			6		
0			1		0			9		
0			1		1			12		
1			0		0			15		
1			0		1			18		
1			1		0			21		
1			**1**		**1**			**24**		

Table 56. RAMP Register (Slope Setting for BUCK1)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
77	02	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RASD1[1:0]	
BITS 7:2			**Reserved, write 000000 to these bits.**							
DESCRIPTION										
BIT 1			**BIT 0**				**SLEW RATE (mV/µs)**			
0			0				5			
0			1				10			
1			**0**				**12.5**			
1			1				25			

Table 57. BUCK1-4ADIS Register (Active Discharge Settings for BUCK1–BUCK4)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
78	04	R/W	Reserved	Reserved	Reserved	Reserved	SD1 ADIS	SD2 ADIS	SD3 ADIS	SD4 ADIS
BITS 7:4			**Reserved, write 0000 to these bits.**							
DESCRIPTION										
SD1ADIS	0		1: Enable BUCK1 active discharge. **0: Disable BUCK1 active discharge.**							
SD2ADIS	1		**1: Enable BUCK2 active discharge.** 0: Disable BUCK2 active discharge.							
SD3ADIS	0		1: Enable BUCK3 active discharge. **0: Disable BUCK3 active discharge.**							
SD4ADIS	0		1: Enable BUCK4 active discharge. **0: Disable BUCK4 active discharge.**							

Note: *The SD3ADIS and SD4ADIS bits are not used by the MAX8982X.*

Table 58. LDO1-8ADIS Register (Active Discharge Settings for LDO1–LDO8)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
79	00	R/W	LDO1 ADIS	LDO2 ADIS	LDO3 ADIS	LDO4 ADIS	LDO5 ADIS	LDO6 ADIS	LDO7 ADIS	LDO8 ADIS
DESCRIPTION										
LDO1ADIS	0		1: Enable LDO1 active discharge. **0: Disable LDO1 active discharge.**							
LDO2ADIS	0		1: Enable LDO2 active discharge. **0: Disable LDO2 active discharge.**							
LDO3ADIS	0		1: Enable LDO3 active discharge. **0: Disable LDO3 active discharge.**							
LDO4ADIS	0		1: Enable LDO4 active discharge. **0: Disable LDO4 active discharge.**							
LDO5ADIS	0		1: Enable LDO5 active discharge. **0: Disable LDO5 active discharge.**							
LDO6ADIS	0		1: Enable LDO6 active discharge. **0: Disable LDO6 active discharge.**							
LDO7ADIS	0		1: Enable LDO7 active discharge. **0: Disable LDO7 active discharge.**							
LDO8ADIS	0		1: Enable LDO8 active discharge. **0: Disable LDO8 active discharge.**							

Note: *The LDO8ADIS bit is not used by the MAX8982X.*

Table 59. LDO9ADIS Register (Active Discharge Setting for LDO9)

ADDRESS (HEX)	POR (HEX)	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
7A	00	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO9 ADIS
BITS 7:1			**Reserved, write 0000000 to these bits.**							
DESCRIPTION										
LDO9ADIS	0		1: Enable LDO9 active discharge. **0: Disable LDO9 active discharge.**							

Applications Information

Inductor Selection

The step-down converters operate with inductors of 1µH to 4.7µH. Low inductance values are physically smaller, but require faster switching, which results in some efficiency loss. The inductor's DC current rating only needs to match the maximum load current of the application plus 100mA because the step-down converters feature zero current overshoot during startup and load transients.

For optimum voltage positioning load transients, choose an inductor with DC series resistance in the 30mΩ to 100mΩ range. For higher efficiency at heavy load (above 200mA) or minimal load regulation (but some transient overshoot), the resistance should be kept below 100mΩ. For light load applications up to 200mA, a higher resistance is acceptable with very little impact on performance.

Recommended inductors are listed in Table 60.

Table 60. Recommended Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	DC RESISTANCE (Ω typ)	CURRENT RATING (mA) ΔT = +40°C RISE	DIMENSIONS L x W x H (mm)
TOKO	MDT2520-CR	1.0	0.06	1550	2.5 x 2.0 x 1.0
		1.5	0.08	1400	
		2.2	0.09	1350	
		3.3	0.10	1300	
	DE2810C Flat Wire	1.5	0.06	2000	3.0 x 2.8 x 1.0
		2.2	0.085	1600	
		3.3	0.130	1300	
		4.7	0.180	1100	
	DE2812C Flat Wire	1.5	0.050	2600	3.0 x 2.8 x 1.2
		2.0	0.067	2300	
		3.3	0.100	1700	
		4.7	0.130	1500	
	DEM3518C	2.2	0.040	2550	3.9 x 3.7 x 1.8
	DEM2818C*	2.2	0.039	2200	3.0 x 3.0 x 1.8
Hitachi-Metals	KSLI-252010AG	1	0.050	2600	2.5 x 2.0 x 1.0
		2.2	0.100	1800	
		3.3	0.100	1800	
		4.7	0.115	1700	
	KSLI-201610AG	1	0.090	1900	2.0 x 1.6 x 1.0
		2.2	0.140	1500	
		3.3	0.180	1300	
		4.7	0.200	1300	
	KSLI-201210AG	1	0.120	1500	2.0 x 1.2 x 1.0
		2.2	0.190	1300	
		3.3	0.230	1200	
		4.7	0.270	1100	
	KSLI-252012AG-2R2**	2.2	0.1	1900	2.5 x 2.0 x 1.2

Table 60. Recommended Inductors (continued)

MANUFACTURER	SERIES	INDUCTANCE (µH)	DC RESISTANCE (Ω typ)	CURRENT RATING (mA) ΔT = +40°C RISE	DIMENSIONS L x W x H (mm)
FDK	MIPF2520D	1.5	0.070	1500	2.5 x 2.0 x 1.0
		2.2	0.080	1300	
		3.3	0.100	1200	
		4.7	0.110	1100	
	MIPF2016D***	1.5	0.110	1100	2.0 x 1.6 x 1.0
		2.2	**0.110**	**1100**	
		3.3	0.130	1000	
		4.7	0.160	900	
	MIPF2012D	1.0	0.090	1100	2.0 x 1.2 x 1.0
		2.2	0.230	700	
		3.3	0.190	800	
		4.7	0.230	700	
Murata	LQM2HP_G0	1.0	0.055	1500	2.5 x 2.0 x 1.0
		2.2	0.80	1300	
		3.3	0.100	1200	
		4.7	0.110	1100	
	LQM21P	1.0	0.190	800	2.0 x 1.25 x 0.50
		1.5	0.260	700	
		2.2	0.340	600	
	LQM2MPN***	1.0	0.085	1400	2.0 x 1.6 x 1.0
		2.2	0.110	1200	
		3.3	0.120	1200	
		4.7	0.140	1100	
Taiyo Yuden	NR3015T1R0N***	1.0	0.030	2100	3.0 x 3.0 x 1.5
	CKP2520	1.0	0.080	1400	2.5 x 2.0 x 1.0
		2.2	0.090	1300	
		3.3	0.120	1200	
		4.7	0.150	1100	
TDK	MLP2520S2R2M	2.2	0.090	1000	2.5 x 2.0 x 1.0
	MLP2520S_S	1.0	0.080	1500	2.5 x 2.0 x 1.2
		2.2	0.110	1200	
		4.7	0.110	1000	
Samsung Electro-Mechanics	CIG22L_	1.0	0.060	1500	2.5 x 2.0 x 1.0
		2.2	0.080	1300	
		3.3	0.100	1200	
		4.7	0.110	1100	
	CIG21W_	1.0	0.130	1050	2.0 x 1.25 x 1.0
		2.2	0.200	810	
		3.3	0.250	730	
		4.7	0.300	650	

**Recommended for BUCK4.*
***Recommended for BUCK1.*
****Recommended for BUCK2 and BUCK3.*

Output Capacitor Selection

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. Recommended capacitor values are shown in Figures 1 and 2.

Input Capacitor Selection

The input capacitor, $C_{IN1\_}$ or $C_{IN\_}$, reduces the current peaks drawn from the input power source and reduces switching noise in the IC. The impedance of C_{IN2} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. Recommended capacitor values are shown in Figures 1 and 2.

PCB Layout Guidelines

Due to fast switching waveforms and high current paths, careful PCB layout is required to achieve optimal performance. Minimize trace lengths between the IC and the inductor, the input capacitor, and the output capacitor for each step-down converter. Keep these traces short, direct, and wide. Route noise sensitive traces away from the switching nodes (LX_).

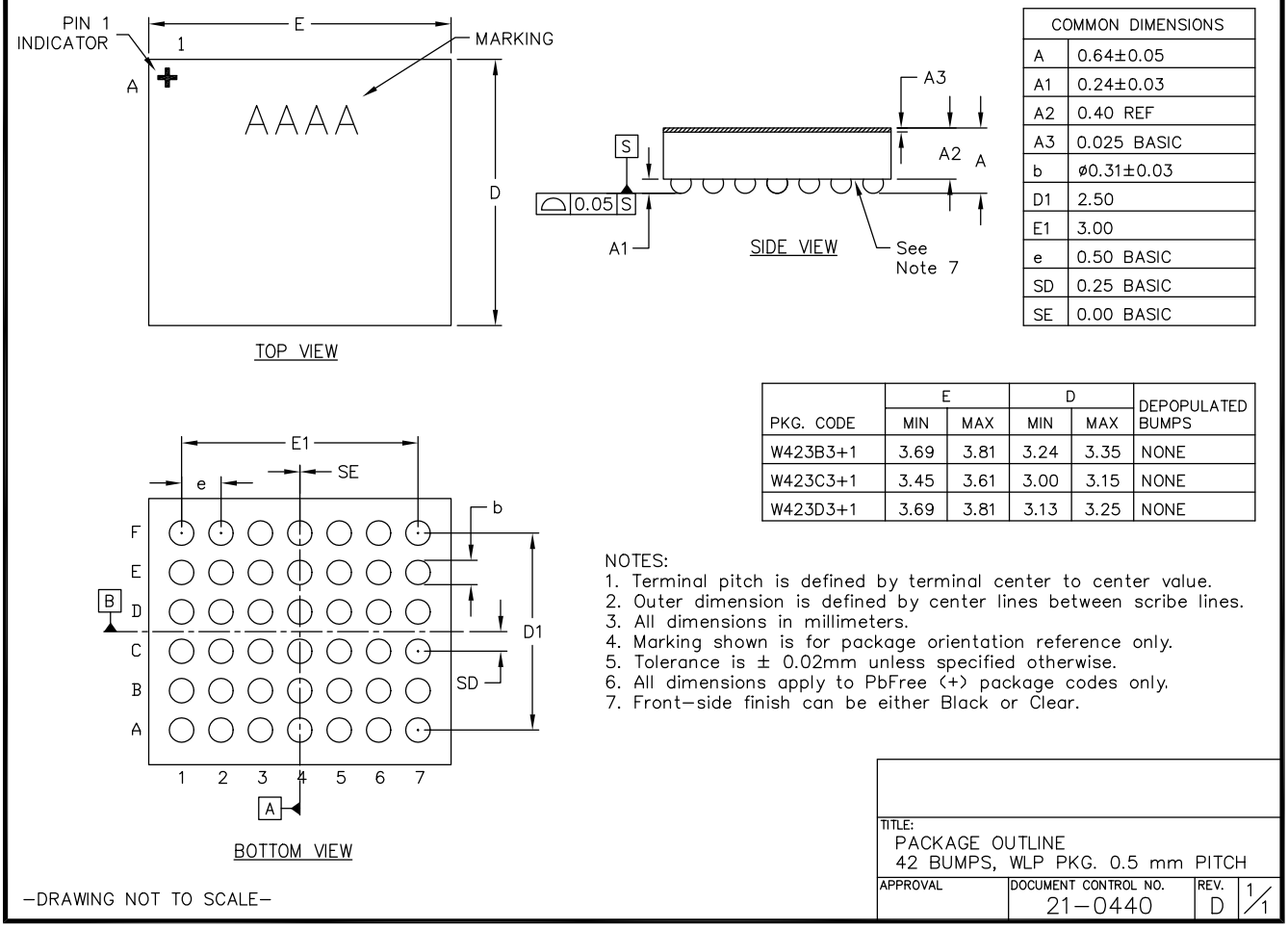
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
42 WLP	W423D3+1	21-0440	Refer to Application Note 1891



COMMON DIMENSIONS	
A	0.64±0.05
A1	0.24±0.03
A2	0.40 REF
A3	0.025 BASIC
b	ø0.31±0.03
D1	2.50
E1	3.00
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W423B3+1	3.69	3.81	3.24	3.35	NONE
W423C3+1	3.45	3.61	3.00	3.15	NONE
W423D3+1	3.69	3.81	3.13	3.25	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front–side finish can be either Black or Clear.

TITLE: PACKAGE OUTLINE 42 BUMPS, WLP PKG. 0.5 mm PITCH			
APPROVAL	DOCUMENT CONTROL NO. 21–0440	REV. D	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—
1	1/11	Added 42 WLP package diagram	72
2	4/11	Added MAX8982P to data sheet and removed references to E450	1–72